Single-Power-Supply Six-Transistor CMOS SRAM Enabling Low-Voltage Writing, Low-Voltage Reading, and Low Standby Power Consumption

Tadayoshi ENOMOTO†, Fellow and Nobuaki KOBAYASHI††, Member

SUMMARY We developed a self-controllable voltage level (SVL) circuit and applied this circuit to a single-power-supply, six-transistor complementary metal-oxide-semiconductor static random-access memory (SRAM) to not only improve both write and read performances but also to achieve low standby power and data retention (holding) capability. The SVL circuit comprises only three MOSFETs (i.e., pull-up, pull-down and bypass MOSFETs). The SVL circuit is able to adaptively generate both optimal memory cell voltages and word line voltages depending on which mode of operation (i.e., write, read or hold operation) was used. The write margin (\(V_{\text{WM}}\)) and read margin (\(V_{\text{MR}}\)) of the developed (dvlp) SRAM at a supply voltage (\(V_{\text{DD}}\)) of 1 V were 0.470 and 0.1923 V, respectively. These values were 1.309 and 2.093 times \(V_{\text{WM}}\) and \(V_{\text{MR}}\) of the conventional (conv) SRAM, respectively. At a large threshold voltage (\(V_t\)) variability (\(=+6\sigma\)), the minimum power supply voltage (\(V_{\text{Min}}\)) for the write operation of the conv SRAM was 0.37 V, whereas it decreased to 0.22 V for the dvlp SRAM. \(V_{\text{Min}}\) for the read operation of the conv SRAM was 1.05 V when the \(V_t\) variability (\(=-6\sigma\)) was large, but the dvlp SRAM lowered it to 0.41 V. These results show that the SVL circuit expands the operating voltage range for both write and read operations to lower voltages. The dvlp SRAM reduces the standby power consumption (\(P_{\text{STBY}}\)) while retaining data. The measured \(P_{\text{STBY}}\) of the 2-kbit, 90-nm dvlp SRAM was only 0.957 \(\mu\)W at \(V_{\text{DD}} = 1.0\) V, which was 9.46% of \(P_{\text{STBY}}\) of the conv SRAM (10.12 \(\mu\)W). The Si area overhead of the SVL circuits was only 1.383% of the dvlp SRAM.

key words: complementary metal-oxide-semiconductor (CMOS), static random-access memory (SRAM), write margin, read margin, standby power consumption, leakage current, minimum supply voltage, area overhead, self-controllable voltage level circuit, single power source

1. Introduction

Decreasing the size of the metal-oxide-semiconductor field-effect transistor (MOSFET) not only decreases the threshold voltage (\(V_t\)) but also increases the standard deviation (\(\sigma\)) of \(V_t\) [1]. As a result, the write and read margins are reduced, write and read operations fail at low voltages, and leakage currents increase appreciably.

Conventional (conv) six-transistor (6T) static random-access memory (SRAM) memory cells offer high areal densities, but as the supply voltage decreases, they are unable to simultaneously achieve large write and read margins. A number of techniques have been proposed to improve the write margin and/or read margin at a low supply voltage [2]–[5], as in the examples of a dual-rail SRAM that generates a lower cell-\(V_{\text{DD}}\) with a certain voltage offset with respect to the logic-\(V_{\text{DD}}\) [2], SRAM with an integrated column-based dynamic multi-\(V\) scheme [3], 6T SRAM with a level-programmable word line driver [4], and single-power-supply 6T SRAM with read and write cell stabilizing circuits [5].

An eight-transistor (8T) SRAM memory cell, which comprised the original 6T SRAM memory cell and two additional MOSFETs [6]–[9], has alternatively been proposed. Reports of 8T SRAM memory cells included 8T SRAM having a dual-port memory cell with two pairs of parallel pass gates [6], cross-point 8T SRAM with negative bias read/write assist [7], 8T SRAM with a 2T read stack sense amplifier for read only [8], and 8T SRAM with a memory cell adopting sense-amplifier redundancy [9]. Regardless of which of the above methods is used, the use of an 8T memory cell leads to an area penalty (i.e., a low area density).

To solve the above problems, we developed a new circuit called the self-controllable voltage level (SVL) circuit and implemented it in single-power-supply, 6T, 90-nm, 2-kbit complementary metal-oxide-semiconductor (CMOS) SRAM. The SVL circuit comprises only three MOSFETs, namely pull-up, pull-down, and bypass MOSFETs. The SVL circuit quickly steps down the externally supplied voltage (\(V_{\text{DD}}\)) and supplies this stepped-down voltage to the memory cells during writing and to the word line drivers during reading. The features of the developed (dvlp) SRAM equipped with this SVL circuit are (1) the low-voltage write and read, (2) the large write and read margins, (3) data retention during standby, and (4) low leakage current during standby.

The present study found that the write margin (\(V_{\text{WM}}\)) of the dvlp SRAM at \(V_{\text{DD}} = 1.0\) V was 0.470 V, which was 1.309 times \(V_{\text{WM}}\) (\(=0.359\) V) of conv SRAM. The read margin (\(V_{\text{MR}}\)) of the dvlp SRAM at \(V_{\text{DD}} = 1.0\) V was 0.1923 V, which was 2.093 times \(V_{\text{MR}}\) (\(=0.0919\) V) of the conv SRAM. The SVL circuit is an effective means of increasing the write and read margins. The minimum power supply voltage (\(V_{\text{Min}}\)) at which data were written to the conv SRAM was 0.37 V when the threshold voltage (\(V_t\)) variability was extremely large (\(=+6\sigma\)). In contrast, \(V_{\text{Min}}\) of the dvlp SRAM (applied with the SVL circuit) decreased to 0.22 V. For very large \(V_t\) variability (\(=-6\sigma\)), the min-
Fig. 1 Developed single-power-supply, six-transistor, 2k-bit SRAM with the built-in self-controllable voltage level (SVL) circuits.

minimum supply voltage \( (V_{\text{MinR}}) \) at which data were read was 1.05 V for conv SRAM and 0.41 V for dvlp SRAM. The dvlp SRAM reduced the standby power consumption \( (P_{\text{ST}}) \) while retaining data. \( P_{\text{ST}} \) of the dvlp SRAM measured at \( V_{\text{DD}} = 1.0 \) V was only 0.957 \( \mu \)W, which is 9.46% of \( P_{\text{ST}} \) of the conv SRAM (10.12 \( \mu \)W). The area overhead of the SVL circuit was 1.383% relative to the dvlp SRAM area. These results demonstrate that the SVL circuit improves margins \( (V_{\text{MW}} \) and \( V_{\text{MR}}), \) lowers minimum power supply voltages \( (V_{\text{MinW}} \) and \( V_{\text{MinR}}), \) and reduces \( P_{\text{ST}} \).

In the following, we describe the structure and operation of the dvlp SRAM with SVL circuits applied (Sect. 2) and the write, read, and standby mode characteristics of conv and dvlp SRAMs (Sects. 3, 4, and 5).

2. SRAM Structure and Operation

2.1 Structure of the Developed SRAM

Figure 1 shows the circuit configuration of the dvlp single-power-supply 6T, 2k-bit CMOS SRAM. This SRAM includes a memory cell array (8 bits \( \times 4 \) words \( \times 64 \) words), self-controllable voltage level (SVL) circuits for the memory cell array (M-SVLs), an SVL circuit for word line drivers (W-SVL), an SVL circuit controller (SVL-C), and peripheral circuits. There are eight M-SVLs in total, one for each 256-bit (8 bits \( \times 4 \) words \( \times 8 \) words) memory cell array, which supply power \( (V_{\text{M}}) \) to the memory cell array. One W-SVL is included to supply power \( (V_{\text{W}}) \) to the word line drivers.

Figure 2(a) shows a 2.5 \( \times \) 2.5-mm\(^2\) prototype chip made using 90-nm CMOS technology. It includes the dvlp SRAM and a conv SRAM (without M-SVLs, the W-SVL and the SVL-C). Figure 2(b) presents the layout of the dvlp SRAM. The silicon areas of the conv SRAM and dvlp SRAM are 65,365 and 66,269 \( \mu \)m\(^2\), respectively. The area overhead of the M-SVLs, W-SVL, and SVL-C is 1.383% relative to the dvlp SRAM area.

2.2 Circuit Diagram

A Conventional SRAM

Figure 3 shows the memory cell and word line driver in the conv SRAM. The memory cell comprises inverter 0 (INV0), inverter 1 (INV1), and two path gates (G0 and G1). U0 and U1 are pMOSFETs, whereas D0, D1, G0, and G1 are nMOSFETs. PS1 and PS2 are the power terminals for the word line driver and memory cell, respectively.

B Developed SRAM

Figure 4 shows the memory cell, word line driver, M-SVL, W-SVL, and SVL-C of the dvlp SRAM. The memory cell structure of the dvlp SRAM is the same as that of the conv
SRAM. PS3 is the power terminal for the dvlp SRAM.

M-SVL comprises a pull-up pMOSFET (pSm) that boosts the memory cell supply voltage ($V_M$) of the dvlp SRAM, a pull-down nMOSFET (nSm) that steps down $V_M$, and a bypass pMOSFET (pSmd) that discharges $C_m$. $C_m$ is the stray capacitance of 256 memory cells seen from M-SVL (point M).

W-SVL comprises a pull-up pMOSFET (pSw) that boosts the word line driver supply voltage ($V_W$) of the dvlp SRAM, a pull-down nMOSFET (nSw) that steps down $V_W$, and a bypass nMOSFET (nSwd) that discharges $C_w$. $C_w$ is the stray capacitance of eight-word line drivers seen from W-SVL (point W).

SVL-C is an on-chip circuit that comprises a small number of logic gates and generates three control signals and two discharge pulses from two input signals and a clock pulse ($\phi_i$). Inputs are the hold control signal ($H$) and read/write control signal ($RW$). Outputs are the control signal ($C_m$) and discharge pulse ($pD_m$) for M-SVL and the control signal ($nC_w$, $pC_w$) and discharge pulse ($nD_w$, $pD_w$) for W-SVL. SVL-C inputs, SVL-C outputs, $V_M$ and $V_W$ are shown in Figs. 5 and 6 in the next section.

Fig. 4  Memory cell, word line driver, M-SVL, W-SVL, and SVL-C in the developed SRAM.

Fig. 5  Three operating modes (write, read, and hold modes) of the developed SRAM and the voltages generated by the M-SVL and W-SVL.
ENOMOTO and KOBAYASHI: SINGLE-POWER-SUPPLY 6T CMOS SRAM ENABLING LOW-VOLTAGE WRITING AND READING, AND LOW STANDBY POWER

469

Fig. 6 Voltage waveforms at each node of the developed SRAM. (a) Clock pulse (\(\phi_i\)). (b) pSmd control pulse (pDm). (c) Voltage supply to memory cells (V_M). (d) nSwd control pulse (nDw). (e) Voltage supply to the word line driver (V_W). (f) Word line voltage (V_Wrd).

Table 1 Voltage (V_M) supplied to the memory cell by M-SVL, control signal 0/1 state (Cm, pDm), and MOSFET on/off state (pSm, nSm, pSmd)

<table>
<thead>
<tr>
<th>Mode</th>
<th>V_M</th>
<th>Cm</th>
<th>pSm</th>
<th>nSm</th>
<th>pDm</th>
<th>pSmd</th>
</tr>
</thead>
<tbody>
<tr>
<td>Write</td>
<td>V_DD−v_nm</td>
<td>1</td>
<td>off</td>
<td>on</td>
<td>0</td>
<td>on</td>
</tr>
<tr>
<td>Read</td>
<td>V_DD</td>
<td>0</td>
<td>on</td>
<td>off</td>
<td>1</td>
<td>off</td>
</tr>
<tr>
<td>Hold</td>
<td>V_DD−v_nm</td>
<td>1</td>
<td>off</td>
<td>on</td>
<td>0</td>
<td>on</td>
</tr>
</tbody>
</table>

Table 2 Voltage (V_W) supplied by W-SVL to the word line driver, control signal 0/1 state (pCw, nCw, nDw) and MOSFET on/off state (pSw, nSw, nSwd)

<table>
<thead>
<tr>
<th>Mode</th>
<th>V_W</th>
<th>pCw</th>
<th>pSw</th>
<th>nCw</th>
<th>nSw</th>
<th>nDw</th>
<th>nSwd</th>
</tr>
</thead>
<tbody>
<tr>
<td>Write</td>
<td>V_DD</td>
<td>0</td>
<td>on</td>
<td>0</td>
<td>off</td>
<td>0</td>
<td>on</td>
</tr>
<tr>
<td>Read</td>
<td>V_DD−v_sw</td>
<td>1</td>
<td>off</td>
<td>1</td>
<td>on</td>
<td>1</td>
<td>on</td>
</tr>
<tr>
<td>Hold</td>
<td>0</td>
<td>1</td>
<td>off</td>
<td>0</td>
<td>off</td>
<td>1</td>
<td>on</td>
</tr>
</tbody>
</table>

2.3 Operating Modes of the Developed SRAM and Voltage Generated by the SVL Circuit

The dvlp SRAM has three modes of operation, namely write, read, and hold (standby) modes. Figure 5 (a) and (b) shows the operating modes of M-SVL and W-SVL, respectively. Also shown are the M-SVL and W-SVL output voltages (V_M and V_W) and the 0/1 states of the input and output signals of SVL-C. Tables 1 and 2 summarize V_M and V_W for the three SRAM operating modes. These tables contain 0/1 states of control signals and on/off states of MOSFET. Figure 6 shows the voltage waveforms of the dvlp SRAM at various nodes. Figure 6 (a), (b), (c), (d), (e), and (f) respectively presents the clock pulse (\(\phi_i\)), pSmd control pulse (pDm), memory cell supply voltage (V_M), nSwd control pulse (nDw), word line driver supply voltage (V_W), and word line voltage (V_Wrd).

A Write Mode

With the control signal (Cm) set to 1, pSm turns off and nSm turns on (Table 1). The voltage (V_M) generated by M-SVL is set to (V_DD−v_nm), when the write mode begins (Fig. 5 (a), Fig. 6 (c)). Here, (V_DD−v_nm) is the voltage drop of 256 memory cells seen from point M, V_DD is the supply voltage to M-SVL (terminal PS3), and v_nm is the voltage drop of nSm.

When the write mode starts, the voltage (V_W) generated by W-SVL is set to V_DD by turning pSw on and nSw off with the control signals (pCw and nCw) set to 0 (Table 2, Fig. 5 (b), Fig. 6 (e)). Thus, the word line voltage (V_Wrd) for the selected word line is set to V_DD (Fig. 6 (f)).

B Read Mode

With Cm set to 0, pSm turns on and nSm turns off. V_M is
Finally, $V_{W}$ charge accumulated in $C_w$ is quickly discharged when changing from the read mode to the write or hold mode. Here, $(V_{DD} - V_{in})$ is the voltage drop of eight clock drivers seen from point $W$ and $V_{in}$ is the voltage drop of $nS$.

C Hold Mode

As well as the write mode with $C_m$ set to 1, $pS_m$ turns off and $nS_m$ operates [Table 1, Fig. 5 (a)]. $V_m$ is set to $(V_{DD} - V_{in})$ when the hold mode begins [Fig. 6 (c)]. Meanwhile, $V_w$ is set to 0 V by turning off $pS_w$ and $nS_w$ when the hold mode starts [Table 2, Figs. 5 (b) and 6 (e)]. This not only results in data being held (stored) but also reduces leakage current (i.e., reduces standby power consumption).

2.4 Effects of Bypass Switches in SVL Circuits

A M-SVL Operation

When changing from the read mode to the write or hold mode, the voltage supplied to the memory cell ($V_m$) must be quickly stepped down from $V_{DD}$ to $(V_{DD} - V_{in})$. However, SRAM with an M-SVL, in which the bypass switch to discharge $C_m$ was not installed [10, 11], took a long time to step down $V_m$. The reason for this is that stored charge in the large $C_m$ had to be discharged through a large equivalent resistance ($R_m$). Here, $R_m$ is the equivalent resistance of the memory cell viewed from point $M$.

To solve the above problem, a bypass switch ($pS_m$) for the quick discharge of $C_m$ was installed in parallel with $C_m$ (Fig. 4). First, we set the control signal ($C_m$) to 1 to turn on $nS_m$. Next, when the control signal ($pD_m$) is set to 0 for a short time [Table 1, Fig. 6 (b)], $pS_m$ is temporarily turned on, and the charge in $C_m$ is rapidly discharged [Fig. 6 (c)]. Finally, $V_m$ converges quickly to the voltage $(V_{DD} - V_{in})$ determined by the resistor values of $nS_m$ and $R_m$.

B W-SVL Operation

In the transition from the write mode to the read mode, the voltage supplied to the word line driver ($V_w$) is stepped down from $V_{DD}$ to $(V_{DD} - V_{in})$. As with the setting of $V_m$ described above, because the charge in the large $C_w$ must be discharged through the large equivalent resistance ($R_w$) seen from point $W$, it takes a long time to step down $V_w$.

To step down $V_w$ rapidly, a bypass switch ($nS_w$) with the same function as $pS_m$ in the M-SVL circuit is installed in parallel with $C_w$ (Fig. 4). First, we set the control signals ($nC_w$ and $pC_w$) to 1 to turn on $nS_w$ and turn off $pS_w$. Next, when the control signal ($nD_w$) is set to 1 for a short time [Table 2, Fig. 6 (d)], $nS_w$ is briefly turned on, and the charge accumulated in $C_w$ is quickly discharged [Fig. 6 (e)]. Finally, $V_w$ rapidly converges to the voltage $(V_{DD} - V_{in})$ determined by the resistance values of $nS_w$ and $R_w$.

Similarly, when changing from the read mode to hold mode, $V_w$ is stepped down from $(V_{DD} - V_{in})$ to 0 V. $V_w$ is also stepped down from $V_{DD}$ to 0 V when changing from the write mode to hold mode. We first set $nC_w$ to 0 and $pC_w$ to 1 to turn off $nS_w$ and $pS_w$. We next set $nD_w$ momentarily to 1 (Table 2, Fig. 6 (d)) and turn on $nS_w$ briefly to quickly discharge the charge stored in $C_w$. Finally, $V_w$ becomes 0 V (Fig. 6 (e)).

3. Characteristics of the Write Mode

3.1 Write Margin

Figure 7 shows the relationship between the static write margin ($V_{WMD}$) and the supply voltages ($V_{DD}$, $V_{DM}$, and $V_{DD}$) applied to the power supply terminals (PS1, PS2, and PS3) ($T = 25^\circ$C, zero $V_t$ variability). The write margin ($V_{WMD}$) was obtained via the following procedure using SPICE. First, $V_{DD}$, $V_{DM}$, and $V_{DD}$ were set to given values $(V_D)$ and $V_{DL}$ was fixed to 0 V, and the transfer characteristics ( $V_{NO}$ vs $V_{NI}$) of INV0 and INV1 were obtained. The transfer characteristics were then superimposed to create a butterfly curve. Finally, $V_{WMD}$ was defined as the length of the square that touches the eye of the butterfly curve.

The solid line, dashed line, and dash-dotted line in Fig. 7 show the write margin of the dvlp SRAM ($V_{WMD}$), the write margin of the conv SRAM ($V_{WMC}$), and the write margin ratio ($V_{WMD}$/ $V_{WMC}$), respectively. The nMOSFET threshold voltage ($V_{n}$) and pMOSFET threshold voltage ($V_{p}$) respectively have mean values of 0.222 V and −0.241 V. The threshold voltage ($V_t$) variability in this case is defined as zero (Table 3).

$V_{WMD}$ is always greater (better) than $V_{WMC}$ when $V_{DD}$
is 0.01 V or higher. For example, when \( V_{DD} = 1 \) V, \( V_{WMD} \) and \( V_{WMC} \) are respectively 0.470 and 0.359 V; i.e., \( V_{WMD} \) is 1.309 times larger (better) than \( V_{WMC} \) [12], [13]. This is explained by the M-SVL stepping down the memory cell supply voltage \( V_M \) to \( (V_{DD} - V_{DD}) \). Similarly, even with large \( V_t \) variability (= +6σ and −6σ), \( V_{WMD} \) is higher than \( V_{WMC} \).

### 3.2 Write Access Time

Figure 8 shows the relationship between the write access time \( (t_W) \) and power supply voltages \( (V_{DW}, V_{DM}, \) and \( V_{DD} \)) obtained in SPICE analysis \( (T = 25^\circ C, \) zero \( V_t \) variability). Note that \( t_W \) is defined as the time from when the address is latched to when the N0 node potential \( (V_{N0}) \) and N1 node potential \( (V_{N1}) \) change by 50%. The solid line and dashed line show \( t_W \) of the dvlp SRAM \( (t_{WD}) \) and \( t_W \) of the conv SRAM \( (t_{WC}) \), respectively. The minimum writable supply voltage \( (V_{MinW}) \) is 0.11 V for the conv SRAM and 0.10 V for the dvlp SRAM. When \( V_{DD} = 0.11 \) V or higher, \( t_{WD} \) is approximately 10% shorter (faster) than \( t_{WC} \). This is explained in that \( V_S \) is stepped down to \( (V_{DD} - V_{DD}) \) by M-SVL, similar to the reason why \( V_{WMD} \) is always higher than \( V_{WMC} \). For example, at \( V_{DD} = 1 \) V, \( t_{WD} \) (= 280 psec) is 25 psec shorter (8.2% faster) than \( t_{WC} \) (= 305 psec).

When the \( V_t \) variability is −6σ (where \( \sigma \) is the standard deviation) (Table 3), the write access time characteristics \( (t_{WD}, t_{WC}) \) are almost the same as the characteristics when the \( V_t \) variability is zero (Fig. 8). \( V_{MinW} \) is 0.27 V for both the conv SRAM and dvlp SRAM.

Figure 9 shows the relationships between \( t_W \) and \( V_{DW}, V_{DM}, \) and \( V_{DD} \) when the \( V_t \) variability is +6σ (Table 3). In this case, \( V_{MinW} \) of the conv SRAM is 0.37 V, and writing is not possible below 0.36 V. Meanwhile, the dvlp SRAM has \( V_{MinW} \) of 0.22 V, which means that the dvlp SRAM has a wider (improved) writable voltage range than the conv SRAM. That is to say, the SVL circuit is extremely effective in extending \( V_{MinW} \) even when the \( V_t \) variability (= +6σ) is large. This is explained in that \( V_S \) is stepped down to \( (V_{DD} - V_{DD}) \) by M-SVL, and it is seen that M-SVL is extremely effective in extending \( V_{MinW} \).

### 3.3 Data Rewriting Operation

#### A Rewriting Failure Case for Conv SRAM

As mentioned above, conv SRAM fails to write (rewrite) data when \( V_{DD} \) is less than 0.36 V and \( V_t \) variability is as large as +6σ. Figure 10(a) shows the potential waveform of each node of the conv SRAM when \( V_{DW} = V_{DM} \) = 0.36 V. (b) Rewrite success case for conv SRAM at \( V_{DW} = 0.36 \) V and \( V_{DM} \) = 0.24 V. (c) Rewrite success case for dvlp SRAM at \( V_{DD} = 0.36 \) V.

---

**Fig. 8** Write access time \( (t_W) \) versus supply voltages \( (V_{DM}, V_{DW}, \) and \( V_{DD} \)) (obtained in SPICE analysis with \( T = 25^\circ C \) and zero \( V_t \) variability).

**Fig. 9** Write access time \( (t_W) \) versus supply voltages \( (V_{DM}, V_{DW}, \) and \( V_{DD} \)) (obtained in SPICE analysis with \( T = 25^\circ C \) and \( V_t \) variability of +6σ).

**Fig. 10** Potential waveforms at each memory cell node in write mode (SPICE analysis at \( T = 25^\circ C, f_c = 1 \) MHz, and \( V_t \) variability of +6σ). (a) Rewrite failure case for conv SRAM at \( V_{DW} = V_{DM} = 0.36 \) V. (b) Rewrite success case for conv SRAM at \( V_{DW} = 0.36 \) V and \( V_{DM} = 0.24 \) V. (c) Rewrite success case for dvlp SRAM at \( V_{DD} = 0.36 \) V.
The original stored datum is retained as it is, and \( V_{N0} \) and \( V_{N1} \) are not inverted. That is to say, data rewriting has failed.

B Rewriting Success Case for Conv SRAM

Figure 10 (b) shows the potential waveform of each node of the conv SRAM, when \( V_{DW} \) is kept at 0.36 V and only \( V_{DM} \) is stepped down, from 0.36 to 0.24 V (\( T = 25^\circ C \) and \( V_t \) variability of \( +6\sigma \)). \( V_{N0} \) and \( V_{N1} \) are inverted, the original stored datum 0 (\( V_{N0} = 0, V_{N1} = V_{DM} = 0.24 \) V) is rewritten to the new datum 1 (\( V_{N0} = V_{DM} = 0.24 \) V, \( V_{N1} = 0 \)), and the data rewriting is successful. However, this approach requires two separate power supplies, one for the memory cells and one for the word line drivers.

C Rewriting Success Case for Dvlp SRAM

Figure 10 (c) shows the potential waveform of each node of the dvlp SRAM, where \( V_{DD} \) supplied to PS3 is 0.36 V, \( T \) is 25\(^\circ\) C and \( V_t \) variability is \( +6\sigma \). Figure 10 (c) shows that the datum has been successfully rewritten. Furthermore, the shape of the potential waveform at each node in Fig. 10 (c) is exactly the same as that of the conv SRAM (Fig. 10 (b)). This also indicates that the datum has been successfully rewritten. This is because the SVL circuits automatically set the word line driver supply voltage (\( V_W \)) and memory cell supply voltage (\( V_M \)) to 0.36 and 0.24 V (\( \approx V_{DD} - V_{thm} \)), respectively. As mentioned above, the conv SRAM requires two separate power supplies. In contrast, the dvlp SRAM has the advantage of requiring only one power supply.

4. Characteristics of the Read Mode

4.1 Read Margin

Figure 11 shows the relationship between the static read margin (\( V_{RMD} \)) and the supply voltages (\( V_{DW}, V_{DM}, \) and \( V_{DD} \)) applied to the power supply terminals (PS1, PS2, and PS3) (\( T = 25^\circ C \), zero \( V_t \) variability).

The read margin (\( V_{RMD} \)) was also obtained by the following procedure using SPICE. We fix \( V_{DW}, V_{DM}, V_{DD}, \) and \( V_{DLb} \) to a given value (\( V_{DD} \)) and obtain the transfer characteristics (\( V_{N0} \) vs \( V_{N1} \)) of INVO and INV1 (see Figs. 3 and 4). Next, we superimpose the transfer characteristics to obtain the butterfly curve. \( V_{RMD} \) is defined as the length of a square that touches the eye of the butterfly curve.

The solid line, dashed line, and dash-dotted line in Fig. 11 are respectively the developed (dvlp) SRAM read margin (\( V_{RMD} \)), conventional (conv) SRAM read margin (\( V_{RMC} \)), and the read margin ratio (\( V_{RMD}/V_{RMC} \)). \( V_{RMD} \) is much greater (better) than \( V_{RMC} \) when \( V_{DD} \) is greater than 0.08 V. For example, when \( V_{DD} \) is 1 V, \( V_{RMD} \) and \( V_{RMC} \) are respectively 0.1923 and 0.0919 V; i.e., \( V_{RMD}/V_{RMC} \) is 2.093 [12], [13]. In other words, \( V_{RMD} \) is 2.093 times larger (better) than \( V_{RMC} \). This improvement is achieved as a result of W-SVL stepping down the word line driver supply voltage \( V_W \) to (\( V_{DD} - V_{thm} \)). Similarly, even with large \( V_t \) variability (\( \approx +6\sigma \) or \( -6\sigma \)) (Table 3), \( V_{RMD} \) is higher than \( V_{RMC} \).

4.2 Read Access Time

Figure 12 shows the read access time (\( t_R \)) versus supply voltages (\( V_{DW}, V_{DM}, \) and \( V_{DD} \)) obtained from SPICE analysis (\( T = 25^\circ C \), zero \( V_t \) variability). Note that \( t_R \) is defined as the time from when the address is latched until the datum is output to the readout circuit. The solid line and dashed line show \( t_R \) for dvlp SRAM (\( t_{RD} \)) and \( t_R \) for conv SRAM (\( t_{RC} \)), respectively. The minimum readable supply voltage (\( V_{MinR} \)) is 0.14 and 0.17 V for dvlp SRAM and conv SRAM, respectively.

For supply voltages above 0.2 V, \( t_{RD} \) is longer than \( t_{RC} \). For example, with \( V_{DD} = 1 \) V, \( t_{RD} \) is 675 psec, which is longer than \( t_{RC} \) (\( \approx 470 \) psec). This is because the word line voltage (\( V_{Wad} \)) has been stepped down. Meanwhile, \( V_{MinR} \) of dvlp SRAM is 0.14 V, lower than that (= 0.17 V) of conv SRAM. In other words, the readable operating range is extended. This is because \( V_{Wad} \) is stepped down. Note that
t_{RD} can be sped up by increasing the drive capability of the readout circuit.

For \( V_t \) variability of +6\( \sigma \), the read access time characteristics (\( t_{RD} \) and \( t_{RC} \)) are similar to those shown in Fig. 12 for zero \( V_t \) variability. \( V_{\text{MinR}} \) is 0.20 V for both the conv SRAM and dvlp SRAM.

The simulated \( f_{\text{GD}} \) (solid lines) and \( f_{\text{GC}} \) (dotted lines) are plotted as functions of \( V_{\text{DD}}, V_{\text{DM}}, \) and \( V_{\text{DW}} \) in Fig. 13 (at \( V_t \) variability of −6\( \sigma \) and \( T = 25^\circ\C \)). \( V_{\text{MinR}} \) is 0.41 V, which is much lower (i.e., much better) than \( V_{\text{MinR}} = 1.05 \) V of the conv SRAM. This means that the dvlp SRAM has a much wider readable voltage range than the conv SRAM. It is clear that a great improvement in the read characteristics of this dvlp SRAM is achieved by lowering the word line voltage (\( V_{\text{Wrd}} \)).

4.3 Data Reading Operation

A Read Failure Case for Conv SRAM

As mentioned earlier, conv SRAM has \( V_{\text{MinR}} \) of 1.05 V. Therefore, data cannot be read out when \( V_{\text{MinR}} \) is below 1.04 V. Figure 14 (a) shows the simulated voltage levels at various nodes of the conv SRAM when \( V_{\text{DW}} \) and \( V_{\text{DM}} \) supplied to PS1 and PS2 are 1.04 V (at \( T = 25^\circ\C \) and \( V_t \) variability of +6\( \sigma \)). This is an example of reading the stored datum 0 (\( V_{N0} = 0 \) V, \( V_{N1} = 1.04 \) V). However, when the word line (\( V_{\text{Wrd}} \)) is activated, \( V_{N0} \) and \( V_{N1} \) are activated. This means that the wrong datum 1 (\( V_{N0} = 1.04 \) V, \( V_{N1} = 0 \) V) is read out and the read operation fails.

B Read Success Case for Conv SRAM

Figure 14 (b) illustrates the simulated voltage levels at various nodes of the conv SRAM, where \( V_{\text{DW}} \) applied to PS1 is reduced from 1.04 to 0.70 V whereas \( V_{\text{DM}} \) applied to PS2 is set at 1.04 V (\( T = 25^\circ\C \), \( V_t \) variability of +6\( \sigma \)). Here, the stored datum is 0 (\( V_{N0} = 0 \), \( V_{N1} = 1.04 \) V). When the word line (\( V_{\text{Wrd}} \)) is activated, \( V_{N0} \) and \( V_{N1} \) are maintained at their original low level (0 V) and high level (1.04 V). Therefore, lowering \( V_{\text{Wrd}} \) makes the conv SRAM successful in the read operation. However, this technique requires two power supplies, namely \( V_{\text{DM}} \) for the memory cells and \( V_{\text{DW}} \) for the word line drivers.

C Read Success Case for Dvlp SRAM

The dvlp SRAM successfully reads the stored data when the voltage (\( V_{\text{DD}} \)) applied to the terminal (PS3) is 1.04 V (\( T = 25^\circ\C \), \( V_t \) variability of +6\( \sigma \)) (Fig. 14 (c)). The shape of the potential waveform of each node in Fig. 14 (c) is exactly the same as that for the conv SRAM [Fig. 14 (b)]. The conv SRAM requires two power supplies to set the word line voltage (\( V_{\text{DW}} \)) and memory cell voltage (\( V_{\text{DM}} \)) to 0.7 and 1.04 V, respectively. In contrast, the dvlp SRAM requires only one power supply (\( V_{\text{DD}} = 1.04 \) V). This is because the SVL circuit automatically sets the word line driver supply voltage (\( V_{\text{Wrd}} \)) and memory cell supply voltage (\( V_{\text{M}} \)) to 0.7 V (\( = V_{\text{DD}} - V_{\text{Ibw}} \)) and 1.04 V, respectively. It is seen that the SVL circuit is effective in extending the minimum read operation voltage of the single-power-supply SRAM even with large \( V_t \) variability (= +6\( \sigma \)).

5. Power Consumption and Operation Speed

As MOSFETs become smaller, the leakage current (\( I_L \)) and standby power consumption (\( P_{\text{ST}} \)) increase. Figure 15 shows the measured \( P_{\text{ST}} \) of developed (dvlp) SRAM as a function of the supply voltage (\( V_{\text{DD}} \)) at \( T = 25^\circ\C \). This \( P_{\text{ST}} \) includes \( P_{\text{ST}} \) for peripherals that are stopped by clock gating in the SRAM standby period. The range of values obtained for five chips is indicated by error bars. The
We developed a single-power-supply, 90-nm, 6T, 2-kbit CMOS SRAM equipped with a newly proposed self-controllable voltage level (SVL) circuit comprising only three MOSFETs. The newly developed (dvlp) SRAM (1) provides larger write and read margins, (2) writes and reads data at low voltages, (3) retains data during standby, and (4) reduces standby power consumption.

The write margin ($V_{WM}$) and read margin ($V_{KM}$) of the dvlp SRAM at a supply voltage ($V_{DD}$) of 1 V are 0.470 V and 0.1923 V, respectively. These values are 1.309 and 2.093 times $V_{WM}$ and $V_{KM}$ of the conv SRAM, respectively.

We showed that the minimum writable supply voltage ($V_{MinW}$) for conv SRAM is 0.37 V when the threshold voltage ($V_t$) variability (= $+6\sigma$) is large. Meanwhile, $V_{MinW}$ of the dvlp SRAM drops (improves) appreciably to 0.22 V. The minimum readable supply voltage ($V_{MaxR}$) for conv SRAM is 1.05 V when the $V_t$ variability (= $-6\sigma$) is large. In contrast, $V_{MinR}$ of the dvlp SRAM decreases to 0.41 V. These results demonstrate that the SVL circuit is useful not only for expanding write and read margins but also for further lowering $V_{MinW}$ and $V_{MinR}$.

The dvlp SRAM significantly reduces the standby power consumption ($P_{ST}$) without losing data. $P_{ST}$ of the dvlp SRAM measured at $V_{DD} = 1$ V is only 0.957 $\mu$W, which is 9.46% of $P_{ST}$ of the conv SRAM (10.12 $\mu$W). We thus find that the SVL circuit not only retains data but also appreciably reduces standby power consumption due to leakage current during standby. Furthermore, the area overhead of the SVL circuit is only 1.383% relative to the total area of the dvlp 2-kbit SRAM.

References


ENOMOTO and KOBAYASHI: SINGLE-POWER-SUPPLY 6T CMOS SRAM ENABLING LOW-VOLTAGE WRITING AND READING, AND LOW STANDBY POWER


Tadayoshi Enomoto received a B.E. degree in Electrical Engineering from Nihon University, Tokyo, Japan, in 1968, and M.S. and Ph.D. degrees in Electrical Engineering from Ohio State University, Columbus, Ohio, in 1972 and 1975, respectively. In 1968, he joined Nippon Electric Co. Ltd. (NEC), where he worked on the design of telephone exchanges. He received a four-year Ohio State University (OSU) fellowship in 1970 and was a fellowship student at the OSU Graduate School from 1970 to 1975. He was also a research associate, studying the mechanisms of photoconduction and luminescence in compound semiconductors, at OSU from 1972 to 1975. In 1975, he returned to NEC and joined NEC Central Research Laboratories. From 1975 to 1982, he was involved in the development of analog MOS LSIs (e.g., CCD filters, switched capacitor filters, adaptive equalizers, analog circuit scaling rules, and manufacturing processes). From 1982 to 1986, he worked on a monolithic stacked IC using SOIs, participating in the Japanese national program for three-dimensional ICs. From 1982 to 1992, he worked on CMOS and Bi-CMOS digital LSIs, including the world’s first video signal processor (1987), dictionary search processors using CAMs (1990), and the world’s first vector processor for supercomputers (1991). From 1986 through 1992, he directed NEC System ULSI Research Laboratories in researching digital LSIs (e.g., microprocessors, video signal processors, and vector processors), memories (DRAMs, SRAMs and CAMs), and analog LSIs (A-to-D converters). From 1992 to 2014, he was a full professor at Chuo University, Tokyo, Japan and from 1998 to 2012, he was also an adjunct professor at Nihon University, Tokyo, Japan. He developed many motion-picture encoding algorithms for super-high-definition TVs, a parallel block-level pipeline architecture for high-speed video signal processors, multimedia processors implementing the dynamic voltage and frequency scaling (DVFS) technique, and low-leakage-current and large-read/write-margin CMOS SRAMs. Since 2014, he has been a professor emeritus at Chuo University. His current research interests include the development of microprocessors and memories for the next generation of mobile communication systems, low-power and high-performance technologies of future LSIs essential for digital video communication and online equipment, and high-speed video coding algorithms for future smart phones and ultra-high-definition TVs. Dr. Enomoto has authored three books, co-authored four books and two handbooks, published 120 reviewed technical papers, and approximately 300 oral presentation papers and holds 50 patents in Japan and abroad. He has received awards including the 1992 Best Paper Award of the IEEE Journal of Solid-state Circuits, the Outstanding Achievement Communication Engineers (IEICE) of Japan (1995), the Best Poster Award of the Eighth System LSI Workshop of the IEICE (2004), the IEEE ASP-DAC Design Contest Special Feature Award (2006), the TELECOM System Technology Award of the Telecommunications Advancement Foundation (2006), a Four-year Ohio State University Fellowship (1970-1974), three NEC R&D Awards (1982, 1985 and 1988), and six Chuo University Prominent Research Awards (1994, 1997, 1999, 2002, 2005, and 2007). Dr. Enomoto is presently an IEEE Life Fellow, an IEICE Life Fellow and an adviser of the IEICE Technical Group of Integrated Circuits and Devices (ICD). He was the chairperson of the IEICE Technical Group of ICD (1993-1995), the chairman of the IEICE Technical Group of Electron Devices (1995-1997), and a member of the IEICE Electronics Research Group Steering Committee (1993-1997). He was an associate editor (1991-1995), an advisory member (1993-1997), and a special issue guest editor (1993, 1995, 1996 and 2009) of IEICE Transactions of Electronics. He was an associate editor of the IEEE Transactions on VLSI Systems (1997-1999) and an associate editor of the IEEE Journal of Solid-State Circuits (2000-2003). He was also a member of the committee nominating candidates for the Japan Prize (2007-2016) and an expert commissioner of the Supreme Court of Japan (2008-2012).
Nobuaki Kobayashi received B.E, M.Sc., and Ph.D. degrees in Information Engineering from Chuo University, Tokyo, Japan, in 2004, 2006, and 2011, respectively. From 2006 to 2014 he was an assistant at the Department of Information and System Engineering, Chuo University, Tokyo, Japan, from 2014 to 2016 he was a specially appointed associate professor at Nagaoka University of Technology, Niigata, Japan, and from 2016 to 2019 he was a full-time lecturer at the Department of Precision Machinery Engineering, Nihon University, Chiba, Japan. Since 2019 he has been an associate professor at Nihon University, Chiba, Japan. His current research interests include the development of motion-picture encoding algorithms, low-power and high-speed CMOS LSI technologies, video encoder architectures, CMOS processors and memories for future LSIs, and brain–computer interfaces. He has published 33 reviewed technical papers and 60 oral presentation papers. He received the 2006 IEEE ASP-DAC Design Contest Special Feature Award. He is a member of the IEEE, the Institute of Electronics, Information, and Communication Engineers (IEICE) of Japan and the IEICE Technical Group of Silicon Materials and Device (SDM). He was a member of the IEICE Technical Group of Integrated Circuits (2014-2021), an assistant secretary of the IEICE Technical Group of SDM (2018-2020) and a secretary of SDM (2018-2020). He was also an editorial secretary of special issue of the IEICE Transactions of Electronics (2017, 2019 and 2021) and a member of the IEICE System LSI Workshop.