FOREWORD

Special Section on Low-Power and High-Speed Chips

Low-power, high-speed chips (COOL Chips) encompass a broad range of architectures, applications, methodologies, and usage models and are essential fundamental techniques to realize Green Transformation (GreenX). These technologies are present in AI, IoT, multimedia, digital consumer electronics, mobile, graphics, encryption, robotics, automotive, networking, medical, healthcare, and biometrics. They are based on novel architectures and schemes for single/multi/many-cores, NoC, embedded systems, re-configurable computing, grid, ubiquitous, dependable computing, GALS, and 3D integration. COOL software, which includes parallel schedulers, embedded real-time operating systems, binary translations and compiler issues, and low-power application techniques, is also emerging.

These technologies all aim to reduce power consumption and enhance chip performance. Regardless of their goals, all of industry has been challenged with developing optimal solutions—both hardware and software—for power optimization according to the required performance. In general, to migrate decades' worth of legacy approaches to low-power technology, researchers approach these optimal solutions from the perspective of starting from scratch.

With this in mind, we have been organizing annual COOL Chips conferences since 1998. We celebrated COOL Chips 25 in April 2022. COOL Chips, a sister conference to HOT CHIPS, focuses on all aspects of cool technologies. Approximately 150 individuals attend the conference each year. In addition to regular paper presentations, the conference includes keynotes and invited talks, special topic presentations, posters, and panel discussions. To attract submissions from engineers and researchers in the industry and academia, the program committee bases acceptance on a 3-page extended abstract and a 6-page paper. The conference proceedings include the final presentation slides with the abstract or the paper. Program committee members reviewed each of the 18 submissions for COOL Chips 25 and selected the 12 bests based on technical merit and innovation.

It is our great honor to announce the publication of this special section on Low-Power and High-Speed Chips. The section is devoted to a variety of techniques for COOL Chips. It contains three papers and one brief paper, among four submissions, which cover the performance and power evaluation of the Fugaku system, data transfer optimization for parallel video encoding architecture, a low-latency 8K-video-transmission system, and logic design for hashing to the elliptic curve and pairing.

On behalf of the editorial committee, we would like to express our sincere appreciation to all the authors for their contributions and to all the reviewers for their critical reviewing papers. Lastly, We would like to thank the editorial committee for their work on this special section, especially, secretaries: Prof. Sakamoto and Prof. Kobayashi.

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