Faster SET Operation in Phase Change Memory with Initialization

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SUMMARY In conclusion, an initialization method has been introduced and studied to improve the SET speed in PCM. Before experiment verification, a two-dimensional finite analysis is used, and the results illustrate the proposed method is feasible to improve SET speed. Next, the R-I performances of the discrete PCM device and the resistance distributions of a 64 M bits PCM test chip with and without the initialization have been studied and analyzed, which confirms that the writing speed has been greatly improved. At the same time, the resistance distribution for the repeated initialization operations suggest that a large number of PCM cells have been successfully changed to be in an intermediate state, which is thought that only a shorter current pulse can make the cells SET successfully in this case. Compared the transmission electron microscope (TEM) images before and after initialization, it is found that there are some small grains appeared after initialization, which indicates that the nucleation process of GST has been carried out, and only needs to provide energy for grain growth later.

key words: Phase Change Memory (PCM), SET speed, initialization, transmission electron microscope (TEM)

1. Introduction

Phase Change Memory (PCM) is one of the leading candidates for next generation data storage devices because of the high read/write speed, good scalability, high retention and robust cycle-endurance [1]–[8]. PCM uses the reversible phase change of a chalcogenide material such as Ge2Sb2Te5 (GST) [9]–[20], which is capable of fast and reversible switch between the crystalline phase (SET state) and the amorphous phase (RESET state).

While phase transition processes are well understood and some PCM chips have been manufactured successfully [21]–[25], SET speed has always been an issue for the realization of future fast speed PCM to meet DRAM like applications. Many efforts have been made to realize high speed of PCM such as the confined-cell, the new chemical vapor deposition technology and new operation method [26]–[30]. These studies mainly focus on single cell and microstructure characteristic, methods for improving chip level operation speed have not been well studied for embedded application. On the other hand, Phase Change Memory (PCM) chips are generally operated by current pulses in practical applications, because voltage pulses will bring some unstable factors such as over-operation. Although it has been proven that ultrafast crystallization of GST can be achieved by applying an incubation electrical field [26]. It is not feasible to use voltage pulses with an incubation voltage for the practical application of PCM chips. Therefore, the new method to improve the SET speed was studied from the perspective of practical application. In this paper, an initialization method, which is made of a separate voltage pulse, has been introduced to improve the SET operation speed in PCM. A two-dimensional finite analysis is used to verify the method before experiment, and the results illustrate the proposed method is feasible to improve the speed of SET operation. The R-I performances of the discrete PCM device and the resistance distributions of a 64 M bits PCM test chip with and without the initialization indicate that the SET speed has been greatly improved by the proposed method. Compared the transmission electron microscope (TEM) images, it is found there are some grains for the cell with initialization, which is taken as the major reason for the reduced SET time.

2. Tables, Figures and Equations

The PCM test chip, which consists of one-transistor-and-one-resistor (1T1R) memory cells, is fabricated by 40 nm CMOS technology. The structure of 1T1R memory cell is shown in Fig. 1 (a). The storage cells are T-shape PCM devices with tungsten (W) top-electron contact (TEC) and titanium nitride (TiN) bottom-electron contact (BEC), as shown in Fig. 1 (b). As a heater, the 35 nm BEC is fabricated on a diameter W plug. The GST film deposited on the BEC layer by physical vapor deposition (PVD) is 100 nm. And the TiN layer between the GST film and the W top electron contact (TEC) is the adhesive layer.

Fig. 1 (a) Schematic of the 1T1R memory cell. (b) TEM image of the T-shape PCM device.
3. Paragraphs and Itemizations

Here, an initialization method is considered, which is made of a voltage SET pulse to improve SET speed. Before verifying this method through experiments, a two-dimensional finite analysis using COMSOL Multiphysics is used to analyze the temperature distribution of the PCM cells during the SET operation using a voltage pulse as shown in Fig. 2. The crystallization is based on the JMAK theory [31], as shown in Eq. (1).

\[
\begin{align*}
    x(t) &= 1 - \exp\left[-(kt)^n\right] \\
    k(T) &= \nu \exp\left(-\frac{E_A}{k_BT}\right)
\end{align*}
\]  

(1)

Where \( t \) is the time, \( n \) is the Avrami coefficient, \( \nu \) is the frequency factor, \( E_A \) is the activation energy, \( T \) is the absolute temperature, and \( k_B \) is the Boltzmann constant. The SET operation is consequently simulated from the RESET state of PCM device. It is well known that the grain structure of GST under normal circumstances is face centered cubic structure (FCC) [28]. Therefore, the thermal conductivity 0.57 Wm\(^{-1}\)K\(^{-1}\) (GST grains with FCC) was used in the simulation [28]. Figure 2 (a) shows the temperature distribution with the voltage pulse 3 V, 200 ns. As a comparison, Fig. 2 (b) is the simulation result with the SET current 0.3 mA, 800 ns. It can be seen that the peak temperature for cell with voltage pulse is much lower than that for the cell with SET current pulse. Obviously, the crystallization has not yet occurred. However, it can be found that the crystalline temperature (468 K) has been reached at the shoulder between the BEC layer and the GST layer, which is thought to cause some nucleation of GST. Then, the power required for grain growth to form crystalline channels is bound to be reduced for the increased grains. Therefore, we believe that the initialization method is feasible to increase the speed of SET operation.

Next, the initialization method is used in the test device. Figure 3 (a) shows a basic electrical circuit used to control the phase transition between the amorphous and crystalline states. The SET current pulses can be generated by a high-speed programmable constant current driver chip, and the voltage pulses are directly given by the pulse generator. In the whole test system, DC test is used to the current-voltage (I-V) scanning and sensing the cell resistance, while AC test is applied to carry out the resistance-current (R-I) and resistance-voltage (R-V) tests. The conversion between AC and DC programming paths is used by the switching circuit. The waveform of the voltage across the cell in the test can be monitored by a digital oscilloscope. Figure 3 (b) shows the R-I curves of the PCM cell with the current SET pulses. The initial current amplitude is 0 mA, and the current step is 0.1 mA. The pulse width \( W_{set} \) is 800 ns. The transient voltages across the sample for \( I_{set} = 0.1 \) mA and \( I_{set} = 0.2 \) mA are shown in the inset of Fig. 3 (b). It is found that the voltage across the sample suddenly drops for \( I_{set} = 0.1 \) mA with the corresponding resistance 800k Ohm. It suggests that GST nuclei are formed although the high conductive crystalline region has not occurred. As the current increases, GST nuclei are connected to have electrical shunting paths, and the SET process completed as shown in Fig. 3 (b). An initialization voltage pulse was applied to the same PCM sample in high resistance state (~1.8M Ohm). The voltage pulse height \( V_{set} \) and pulse width \( W_{set} \) were 3.0 V and 200 ns, respectively. After the initialization, the regular R-I tests were performed, for which the pulse height \( I_{set} \), current step and pulse width \( W_{set} \) were 0 mA, 0.1 mA and 500 ns, respectively. The test results were shown in Fig. 3 (c). It is observed that the resistance value after initialization is about 92k Ohm, which is in the middle of high and low resistance. The resistance value is about 20k Ohm for \( I_{set} = 0.1 \) mA, which is much lower than that shown in Fig. 3 (b). The result indicates a faster SET operation since lower pulse amplitude (0.1 mA) and narrower pulse width (500 ns). In the inset of Fig. 3 (c) shows the voltages across the sample for \( I_{set} = 0.1 \) mA and \( I_{set} = 0.2 \) mA. Compared with the waveforms shown in inset of Fig. 3 (b), it is found that there are no voltage suddenly drops for the sample with initialization, which suggests that some nucleation of GST occurred during initialization. This conclusion is consistent with the simulation results shown in Fig. 2. Therefore, GST is at the growth stage in the subsequent R-I tests, which in-

![Fig. 2](image-url) Simulated SET temperature distributions in PCM cells with (a) voltage pulse and (b) current pulse.

![Fig. 3](image-url) (a) Electrical circuit used to control the phase transition between the amorphous and crystalline states. The R-I curves for the PCM sample (b) without and (c) with initialization. Inset in (b) and (c) are the transient voltage waveforms during the R-I tests, respectively.
Fig. 4  The resistance distributions of (a) 3 times repeated initialization for the same test PCM chip without any current SET, and (b) one time initialization for 5 different PCM test chips.

Fig. 5  The SET resistance distributions with and without initialization of the test PCM chip. The optimal initialization used is a 3 V, 200 ns SET pulse. On the top of figure is the schematic of the initialization process.

Fig. 6  (a) The TEM image showing the cross-section of the PCM cell without initialization. (b) The HRTEM image of the areas marked in (a). Inset in (b) is the FFT pattern from the corresponding region marked in (a). (d) The TEM image of the PCM cell after initialization. (c) The HRTEM image of the areas marked in (d).

evitably leads to a faster SET operating speed and lower power consumption.

In order to ensure the stability of the initialization method, we first verified it based on the test chips. The experiment results are collected from the 64 Mb PCM test chips with an Automatic Test Equipment (ATE). The optimal initialization used is a 3 V, 200 ns SET pulse based on the repeated experiments results. As the same RESET pulses are applied to the devices before each SET operation, the RESET resistance are the same. Figure 4 (a) is the resistance distribution of 3 times repeated initialization operations for the same test PCM chip. It shows the basically same initialized resistance distributions, and about 62 percent of the cells’ resistance is between 30 kΩ and 300 kΩ. It suggests that the proposed initial operation method is reliable for the same PCM chip. The initialize experiments for 5 different PCM test chips (Chip No.1 to No. 5) are also carried out as shown in Fig. 4 (b). It also indicates stable initialized resistance distributions with minor variations, and about 59~66 percent of the cells’ resistance are in the range of 30 kΩ~300 kΩ. All the results shown in Fig. 4 (a) and (b) ensure the reliability of subsequent experiments. Obviously, the applied voltage pulse is not enough for the PCM array to achieve SET successfully. But the resistances for a large number of PCM cells have been successfully changed to be in an intermediate state, which is thought that only a shorter current pulse can make the cells SET successfully in this case.

To further investigate the impact of initialization on SET operation, the resistance distributions of the test PCM chip with and without initialization are shown in Fig. 5. The schematic of the complete initialization process is shown on the top of Fig. 5. The current SET conditions without initialization are fixed as 0.3 mA-500 ns and 0.3 mA-1000 ns. It can be seen that only about 69 percent of the cells’ resistance is below 50 kΩ. It means that nearly one-third of the cells have not fully crystallized under 0.3 mA-500 ns. While, about 90 percent of the cells’ resistance is below 50 kΩ with the SET pulse 0.3 mA-1000 ns, which is a good SET resistance distribution result. Compared the SET resistance distributions as shown in Fig. 5, it is also found that the SET distribution of 500 ns SET with initialization is similar to that of 1000 ns SET without initialization. It further proves that the SET speed becomes faster by using the initialization. The chip currently designed is operated in bytes, and it can be calculated that the SET speed of each byte has increased by at least 300 ns. Therefore, the operating speed of the entire chip will be greatly improved.

In order to find out the changes in the cell before and after the pre-operation, the microscopic study of the cells was carried out. The cross sections of the cells are prepared by focused ion beam (FIB). The transmission electron microscope (TEM) image of the cell at RESET state without initialization is presented as shown in Fig. 6 (a). Inset in (b) is the FFT pattern from the corresponding region marked in (a). (d) The TEM image of the PCM cell after initialization. (c) The HRTEM image of the areas marked in (d). And an obvious amorphous region can be iden-


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