A Novel Technique to Suppress Multiple-Triggering Effect in Typical DTSCRs under ESD Stress

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SUMMARY This work reports a new technique to suppress the undesirable multiple-triggering effect in the typical diode triggered silicon controlled rectifier (DTSCR), which is frequently used as an ESD protection element in the advanced CMOS technologies. The technique is featured by inserting additional N-Well areas under the N+ region of intrinsic SCR, which helps to improve the substrate resistance. As a consequence, the delay of intrinsic SCR is reduced as the required triggering current is largely decreased and multiple-triggering related higher trigger voltage is removed. The novel DTSCR structures can alter the stacked diodes to achieve the precise trigger voltage to meet diode trigger conditions. All explored DTSCR structures are fabricated in a 65-nm CMOS process. Transmission-line-pulsing (TLP) and Very-Fast-Transmission-line-pulsing (VF-TLP) test systems are adopted to confirm the validity of this technique and the test results accord well with our analysis.

key words: electrostatic discharge (ESD), transmission-line-pulsing (TLP), very-fast-transmission-line-pulsing (VF-TLP), multiple-triggering, diode-triggered silicon controlled rectifier (DTSCR)

1. Introduction

The diode triggered silicon controlled rectifier (DTSCR) continues an important ESD protection element in the CMOS process owing to its adjustable trigger/holding voltage, low parasitic capacitance, and simplifications [1], [5]. However, this structure has the multiple triggering effect and exhibits a large trigger voltage, which significantly limits its applications in ESD protection for the advanced semiconductor technology [6]. Furthermore, requirements of connecting thin oxide to pads increase as core devices are frequently used as I/O in the high-speed integrated circuits (ICs), and the upper bound of ESD design window is limited to the breakdown of thin gate oxide [7]. Therefore, previous works have proposed many modified DTSCR devices to minimize this phenomenon, in which the parasitic SCR plays an important role [8], [9]. Unfortunately, shortening or lengthening the parasitic SCR path can decrease this effect, but not suppress it.

In this work, embedding N-wells under the N+ area of intrinsic SCR is proposed to solve this puzzle. First of all, the influence of the parasitic SCR on DTSCRs’ ESD behaviors is explored in detail with TCAD tools. It is demonstrated that, the parasitic SCR dominates in ESD current discharging procedure after the turn-on of stacked diodes in the typical DTSCR. Due to a larger part of ESD current passing through the parasitic SCR, the switch-on of the intrinsic SCR is delayed, which results in the multiple triggering phenomenon. Secondly, to weaken parasitic SCR’s influence, additional N-Well areas are inserted under the N+ region of intrinsic SCR to improve substrate resistance, which lowers the triggering current required in the intrinsic SCR. The delay-time of intrinsic SCR is largely reduced, and the multiple triggering phenomenon is suppressed as expected under the TLP test. Besides, under the low identical VF-TLP current, the modified DTSCRs can achieve a much shorter turn-on time than that of the typical one. As the VF-TLP current is raised, this improvement is not so obvious.

2. Exploration and Improvements

Typical DTSCR’s ESD behaviors are influenced by parasitic SCR, which can be observed in the cross-section view depicted in Fig. 1. Under the ESD stress, the diode chain first turns on, then the parasitic SCR, and finally the intrinsic SCR. The first snapback is attributed to the switch-on of the diode chain, and the second snapback comes from the intrinsic SCR. It is obvious that, the parasitic SCR’s turn-on does not cause a similar snapback, which indicates its limited influence on the total resistance modulation. However, parasitic SCR’s current shunting ability must not be neglected due to its significant influence on the intrinsic SCR’s turn-on procedure.

To obtain a deeper insight into this issue, device simulations are performed to show how ΔVBE, labeled in Fig. 1, varies as the DTSCR is turned on under the improved voltage pulse in Fig. 2. The TCAD tools are used to simulate the TLP test procedure. When the applied voltage pulse occurs, the diode chain first turns on to discharge ESD current and then the parasitic PNP’s switch-on results in the first snapback. However, the ΔVBE is too small to switch on the
intrinsic SCR. With the improved voltage pulse, the parasitic SCR is triggered together with a larger current passing through $R_{\text{sub}}$, which leads to an increased $\Delta V_{\text{BE}}$. Eventually, the $\Delta V_{\text{BE}}$ is large enough to switch on BE junction in the NPN BJT, and a low-impedance path is formed in the intrinsic SCR. From Fig. 2, it can be deduced that multiple triggering phenomenon results from the delayed intrinsic SCR. Further, this delay in the intrinsic SCR is attributed to a higher triggering current. Therefore, improving the $R_{\text{sub}}$ can reduce the current required in intrinsic SCR and suppress multiple triggering effect in DTSCR’s turn-on process during an ESD event.

Based on above discussions, additional N-Wells are inserted under the N+ area of intrinsic SCR to achieve an improved $R_{\text{sub}}$. Three devices are taken for example and marked with DTSCR [a], [b] and [c] in Fig. 3, which are characterized with the embedded N-Wells under the N+ region along the full width, half-width in the middle and both sides. The cross-section view of the proposed DTSCR structures are shown in Fig. 4.

For comparison, the width of 10 $\mu$m is selected in all device simulations, which are depicted in Fig. 5 and Fig. 6. When low voltage pulse is applied, the novel DTSCR[a],
DTSCR[b] and DTSCR[c] has a larger $\Delta V_{BE}$ than that in the typical DTSCR due to the embedded N-Wells are located in, which means a less current is required in the engineered intrinsic SCR. When the voltage pulse is switched to a higher level, a larger current density will be formed where the improved $\Delta V_{BE}$ exists in the novel DTSCRs. The distribution of current density shows a little difference along the width due to meshing asymmetry in the device simulations. Together with the increased voltage pulse, the intrinsic SCR will be triggered and switched into a low-impedance state and discharge the majority of ESD current. The improved $R_{sub}$ helps to reduce the intrinsic SCR’s delay and suppress the multiple triggering effect.

### 3. Silicon-Data Verification

A Thermo TLP/VF-TLP test system is used to extract the ESD behaviors of the typical and the proposed DTSCR devices. The TLP test results are depicted in detail in Fig. 7. The multiple triggering effect is observed in typical DTSCR device, but suppressed in the proposed DTSCRs. This is due to the improved $R_{sub}$ in the latter, which is able to lower the current required in the intrinsic SCR and therefore weaken the parasitic SCR’s influence. When the ESD event occurs, the diode chain begins to discharge the ESD current, and then the parasitic PNP BJT results in the first snapback as analyzed. According to the raised $R_{sub}$, the collected current in the collector of the PNP BJT is large enough to turn on the NPN BJT. Thus, the delay in the intrinsic SCR is reduced to such a low level that the multiple triggering effect is suppressed.

The simulated TLP I-V curves are depicted in Fig. 8. However, the first snapback in the typical DTSCR is not observed in this simulation setup due to the nearly unchanged parasitic resistance in the whole device structure, which indicates a very limited influence of the turn-on of the diode.
Fig. 9 VF-TLP I-V curves of the typical and proposed three DTSCRs

Fig. 10 Transient waveforms of the typical and proposed three DTSCRs when the VF-TLP current is (a) 0.8 A and (b) 2 A, respectively.

chain. The obvious second snapback can be achieved owing to the much higher triggering current in the intrinsic SCR, and then be suppressed in the novel DTSCR devices as above discussed.

The VF-TLP tests are also performed using the transient pulses with 150 ps rise time and 5 ns duration. The experimental I-V curves are extracted from the average between 3.75 ns and 4.5 ns as applied pulse is improved, which is illustrated in Fig. 9. The test results show that the proposed three DTSCRs can also obtain a precise trigger voltage about the turn-on potential of four stacked diodes, which is much lower than that of the typical structure. However, on-resistance of the three proposed DTSCRs is slightly higher than that of the typical one, which is according to the lower doping concentration of inserted N-Well areas in the former three devices. This phenomenon is more obvious in the VF-TLP test than in the TLP test.

The transient waveform is drawn in Fig. 10 when the VF-TLP current is 0.8 A and 2 A, respectively. Compared with the typical DTSCR, the novel three DTSCRs exhibit a much shorter turn-on time under the VF-TLP current is 0.8 A, which is attributed to the less delay of the intrinsic SCR with embedded N-Well. When the VF-TLP current is switched to 2 A, the turn-on time is largely reduced and the difference between the typical and proposed DTSCRs becomes small.

4. Discussion

The novel technique proposed in this work can suppress the multiple triggering effect in the DTSCRs, which has achieved better results than the previous works. Besides, no extra design cost is required. Exploration is focused on intrinsic SCR’s modification rather than engineering the parasitic SCR. Furthermore, this technique is useful in removing the multiple triggering effect when the diode number is altered, which has been verified in both the 65-nm and 55-nm CMOS process.

ESD behaviors of modified DTSCRs with the proposed technique may be a little different in advanced CMOS process according to the doping of the N-Well. To our acknowledgement, the holding voltage can be raised by increasing the distance between the anode and cathode in the intrinsic SCR to satisfy the different ESD protection requirements, but related research is beyond the scope of this work.

5. Conclusion

A new technique to suppress the undesirable multiple-triggering effect in the typical DTSCR is reported in this work. Exploration of the parasitic SCR’s influence on the typical DTSCR’s ESD behaviors is performed in detail. Reducing intrinsic SCR’s triggering current by inserting the additional N-Well under the N+ regions is able to improve the substrate resistance to suppress this effect. These DTSCRs were fabricated with a 65-nm CMOS process and investigated with a TLP/VF-TLP system. Device simulations were performed, and these results matched the test.

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References


