A Tunable Dielectric Resonator Oscillator with Phase-Locked Loop Stabilization for THz Time Domain Spectroscopy Systems

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SUMMARY   Precision microwave measurement systems require highly stable oscillators with both excellent long-term and short-term stability. Compared to components used in laboratory instruments, dielectric resonator oscillators (DRO) offer low phase noise with greatly reduced mechanical complexity. To further enhance performance, phase-locked loop (PLL) stabilization can be used to eliminate drift and provide precise frequency control. In this work, the design of a low-cost DRO concept is presented and its performance is evaluated through simulations and measurements. An open-loop phase noise of $-107.2$ dBc/Hz at 10 kHz offset frequency and 12.8 GHz output frequency is demonstrated. Drift and phase noise are reduced by a PLL, so that a very low jitter of under 29.6 fs is achieved over the entire operating bandwidth.

\textit{key words:} dielectric resonator oscillator, phase jitter, phase-locked loop, phase noise, voltage-controlled oscillator

1. Introduction

With ever faster electronics, terahertz spectroscopy is becoming increasingly important for noninvasive materials detection and characterization. Common applications are airport security screening [1], production quality control [2] and bio-sensing [3]. One method to process the large bandwidth is to use the subsampling radar principle by means of asynchronous optical sampling (ASOPS) [4]. Two modelocked laser diodes functioning as pulse generators are operated at slightly offset repetition rates so that they can be used to sample each other [5]. Thus, the obtained IF signal is stretched in the time domain, allowing digitization at moderate frequencies. Typically, the repetition rates are in the microwave regime and generated by local oscillators. These must be highly stable with excellent phase noise to achieve good resolution and accuracy, especially in subsampling systems. The most common and proper approach is using a fundamental oscillator operating at the repetition frequency, which is locked to a highly stable time base, such as an oven-controlled crystal oscillator (OCXO).

Various types of microwave local oscillators exist with different advantages and disadvantages regarding tuning range and stability. LC-based oscillators utilizing a varactor for tuning are most common. Their resonator can be realized either with lumped elements [6] or transmission lines [7], depending on the frequency range and the implementation technology. They are easy to implement and cover a wide frequency range, but achieve only low quality factors and thus exhibit relatively high phase noise as shown by Leeson [8]. In contrast, Yttrium Iron Garnet (YIG) oscillators (YTO) are based on a YIG sphere as resonator. This offers a superb quality factor, which is one to two orders of magnitude higher, while remaining tunable by syntonizing the DC magnetic field through the YIG sphere [9]. However, YIG oscillators exhibit high mechanical complexity, size, and overall power dissipation. Thus, they are less suitable for mobile, low-cost systems. In [9], the phase noise of state-of-the-art wideband tunable oscillators is compared, presenting an LC-VCO with $-80$ dBc at 10 kHz frequency offset over 6.5...15.1 GHz tuning range and a YTO with $-110$ dBc at 10 kHz frequency offset over 6...12 GHz tuning range.

Dielectric resonator oscillators (DRO) offer a reasonable compromise, as they are simple in design and exhibit good phase noise performance at the same time. The resonator consists of a dielectric puck, which is typically made of ceramic material with a high relative permittivity and low dissipation factor, resulting in a high quality factor comparable to YIG. In return, the electronically tunable frequency range is small. However, the puck’s resonance frequency can be tuned by mechanical manipulation of the cavity height, e.g. with screws [10]. This is important to account for varying pulse repetition rates in manufacturing of the laser diodes. Moreover, the electronics can be realized with off-the-shelf components.

The low-cost and compact design makes DROs a good candidate for high-quality fixed-frequency applications like mobile THz time domain spectroscopy systems (THz-TDS). To precisely control the frequency, compensate drifts, as well as decrease phase noise close to the carrier, the DRO can be stabilized by a phase-locked loop (PLL) [11]. Hence, the DRO requires a mechanism to modulate the oscillation frequency by a tuning voltage without degrading the resonator’s quality factor [10]. Therefore, we introduced in [12] a voltage-controlled DRO (VCDRO). In this work, we fully characterize this VCDRO with very low jitter over a wide tuning range and compare it to the simulations.

2. Fundamental Design

The presented DRO is a transmission-type oscillator, as it offers well predictable behavior and suppression of spurious oscillations. The block diagram of the DRO is shown in Fig. 1. Hence, the open-loop gain $A_{OL}$ must satisfy ampli-
tude and phase condition according to Barkhausen:

\[ |A_{OL}| = 1 \quad (1) \]
\[ \arg (A_{OL}) = n \cdot 2\pi, \quad n \in \mathbb{Z} \quad (2) \]

Due to its high \( Q \)-factor, the resonator acts like an extremely narrow bandpass filter with high stopband attenuation and hence suppresses oscillations outside the resonance. The in-loop amplifier compensates for the remaining attenuation at the resonance, as well as additional losses by the other components and lines. The adjustable microstrip line guarantees the phase condition (2) at the desired oscillation frequency. The power splitter and subsequent isolation amplifier are used to extract and decouple the output signal.

Electronically tuning of the resonator’s resonance frequency is possible by different techniques. On the one hand, the electric or magnetic field inside the cavity can be perturbed. For instance, this can be realized by varactor-tuned antennas, magnetically tuned ferrites, or mechanically tuning the cavity using actuators [13]. Although these implementations exhibit a comparably large tuning range, they increase the complexity of the resonator design and either impair the quality factor or offer a small control bandwidth.

On the other hand, the resonance frequency can be slightly tuned by an external phase shift. While this technique barely influences the quality factor and offers a high control bandwidth, it has only a comparably small tuning range. However, the suppression of phase noise requires only a small frequency excursion of the VCDRO. Hence, a varactor-based phase shifter is a proper solution. A branch-line coupler splits the input signal into two paths where it is reflected at a varactor diode and finally recombined by the coupler [14]. This provides a predictable phase shift over a wide operating frequency range and a modular design approach. Given the resonator’s transmission characteristic, the electronic tuning range can be determined and approximately corresponds to the resonator’s 3 dB-bandwidth.

3. Realized Setup

The presented DRO is intended as time base for THz-TDS based on mode-locked laser diodes at a pulse repetition rate at around 12.8 GHz. A proof of concept is demonstrated in [15]. The time base’s jitter must be negligible compared to the laser diode’s pulse width for appropriate measurements. Tolerances in manufacturing of the laser diodes cause variations of the repetition rates, so the DRO’s oscillation frequency must be adjustable over several 100 MHz. As the ASOPS concept requires two signal sources locked to each other with an offset of a few kHz, the PLL-stabilized DRO in Fig. 2 is developed. The setup consists of a fractional PLL board based on the ADF41513, which locks the VCDRO to an external 100 MHz OCXO (Axtal AXIOM5050ULN). The PLL’s tuning voltage is fed to the phase shifter’s varactor diodes (MAVR-011020-1411) on the VCDRO board.

The DC bias voltage is applied to the microstrip line through a \( \lambda/4 \)-stub and fed to the varactors over the coupler. To enable an optimal operation point of the electronic phase shifter, the length of a microstrip line can be adjusted with a short. By means of a Wilkinson divider and the isolation amplifier the DRO’s signal is extracted. The low noise amplifier HMC903 is utilized for both, the in-loop and the isolation amplification. Rogers RO3003™ with a height of 130 \( \mu \)m is used as substrate for all RF structures on the VCDRO board.

The resonator’s dielectric puck is a cylinder with a diameter of 5.3 mm and a height of 1.59 mm made of Exxelia E4000. It is placed 3 mm above the substrate by an alumina spacer and magnetically excited by two microstrip lines in its TE014 mode [16]. The dielectric resonator is enclosed by a brass cavity with an inner diameter of 10 mm. To manually tune the DRO over a wide range of operating frequencies, a tuning screw traverses the cavity’s top cover.

4. Measurements

The dielectric resonator and the phase shifter were assembled on a test PCB to measure their transmission characteristics independently. A TLR calibration with reference planes at the microstrip lines in front of the structures was applied. S-parameter simulations were performed in CST Studio Suite® using the frequency domain solver with a tetrahedral mesh. The transmission \( S_{21} \) of the DR at around 12.82 GHz was measured and simulated, as depicted in Fig. 3. The phase offset \( \Delta \phi \) is normalized to 0° at the resonance frequency.
Fig. 3  Measured and simulated transmission $S_{21}$ of the dielectric resonator represented by magnitude and phase.

The resonator’s $Q$-factor can be determined by the 3 dB-bandwidth of $|S_{21}|$ or by

$$Q = \frac{f_0}{2} \left. \frac{\partial \Delta \varphi}{\partial f} \right|_{f=f_0}$$

resulting in 3562 and 3544, respectively. Deviations of the transmission characteristics from simulation may be caused by small inaccuracies in the loss estimation of materials and surfaces.

Fig. 4 shows the measured transmission $S_{21}$ of the phase shifter at 12.8 GHz over the tuning range of 0 . . .15 V. Insertion loss is between 1.5 dB and 2.5 dB, which is sufficiently low and constant. A maximum phase shift of 83° is achieved. In all further measurements the voltage range was limited to 0 . . .5 V, giving a maximum phase shift of 67°. The adjustable line is used as additional phase shifter, to center the electronic tuning range on the resonator’s passband. This provides the largest frequency deviation with minimal attenuation. After adjusting the microstrip line for optimal tuning range, the tuning characteristic of the oscillator board in Fig. 5 was measured. At a base frequency of 12.8 GHz, the maximum frequency shift is 2.1 MHz, which agrees well with the measurements in Fig. 3 and Fig. 4, giving a theoretical shift of 2.4 MHz. For comparison, the simulated frequency shift is shown by evaluation of the simulated S-parameters of the open oscillator loop with respect to the phase condition (2). However, the validity of the simulation is limited since nonlinear effects of the saturated amplifier are not considered.

The oscillator’s phase noise power spectral density shown in Fig. 6 was measured with connected PLL stabilization for both, open- and closed-loop operation, using a phase noise analyzer (R&S® FSWP). In open-loop operation, the PLL was turned off to retain an identical signal path through the output buffer. The phase noise power spectral density shows the typical shape for an oscillator with a slope of $-30$ dB per decade with respect to the offset frequency, which fades into the noise floor at higher offset frequencies. In this setup, an additional region with $-10$ dB per decade occurs above $\sim 300$ kHz. This is caused by upconversion of noise in the saturated isolation and buffer amplifiers in the oscillator and PLL, respectively. Around 400 Hz offset frequency the influence of electromagnetic interference (EMI) is visible, because the oscillator prototype is not shielded.

Using the measured open-loop phase noise of the components, the PLL’s loop filter is designed for lowest integrated jitter between 100 Hz . . .1 MHz. This results in a loop bandwidth of 16.9 kHz and a high phase margin of 70,6° for the implemented 4th order active filter. As expected, the PLL reduces the phase noise and especially the EMI at offset frequencies $\leq 6$ kHz. However, the noise is increased between 6 kHz . . .500 kHz. This is caused by the PLL chip, which is the major contributor to the closed-loop phase noise, as proofed by the simulations performed in ADIsimPLL™ de-

Fig. 4  Measured and simulated transmission $S_{21}$ of the phase shifter represented by magnitude and phase at 12.8 GHz.

Fig. 5  Measured and simulated tuning characteristic of the DRO at a base frequency of 12.8 GHz.

Fig. 6  Measured phase noise of the DRO in open- and closed-loop operation at 12.8 GHz and simulated noise contributions.
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Fig. 7 Measured open-loop (OL) phase noise at 1 kHz, 10 kHz and
100 kHz offset frequency as well as closed-loop (CL) jitter integrated be-
tween 100 Hz . . . 1 MHz as function of the output frequency.

Picted in Fig. 6. To improve the performance, A PLL with
dedicated high-performance phase frequency detector and
divider [17] can be used.

The performance of the PLL-stabilized DRO is measured over the possible frequency range of 12.74 GHz . . . 13.1 GHz. This corresponds to a bandwidth of 360 MHz or 2.8 %, respectively. The measured open-
loop phase noise at 1 kHz, 10 kHz and 100 kHz offset, as well as the measured closed-loop jitter integrated from 100 Hz . . . 1 MHz are depicted in Fig. 7 as function of the output frequency. Due to higher resonator attenuation and losses introduced by the adjustment screw, the open-loop phase noise increases with the output frequency. In contrast,
the closed-loop jitter is relatively constant, confirming the PLL chip as dominating noise source. With all, the jitter integrated from 100 Hz . . . 1 MHz is not higher than 29.6 fs over the entire tuning range. At its best, the system achieves a small jitter of 27.6 fs, which is in good agreement to the simulated value of 26.3 fs. Output power also remains quite constant in the range 16.9 . . .17.8 dBm. Depending on the output frequency, the oscillator’s amplifiers consumes about 1.08 W . . .1.23 W.

5. Conclusion

A PLL-stabilized DRO is presented for the use as time base in
THz-TDS. The DRO features a manual range selection covering
12.74 GHz . . . 13.1 GHz and an electronic fine tuning for best performance and PLL-stabilization. In open-loop, the DRO achieves −107.2 dBc/Hz at 10 kHz offset and 12.8 GHz carrier, which is just slightly higher than a comparable YTO listed in [9], but still represents a 27 dB improvement over an LC-based oscillator with only minor increase in complexity. In closed-loop, the PLL reduces phase noise close to the carrier, resulting in a jitter as low as 27.6 fs integrated from 100 Hz . . . 1 MHz. Further improvement can be achieved by dedicated PLL components instead of commercial ones.

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