Experimental Exploration of the Backside ESD Impacts on an IC Chip in Flip Chip Packaging

Takuya Wadatsumi†, Member, Kohei Kawai‡, Rikuu Hasegawa†, Kikuo Muramatsu†, Hiromu Hasegawa‡, Takuya Sawada§, Takahito Fukushima§, Hisashi Kondo§, Takuji Miki†, Member and Makoto Nagata†, Senior Member

SUMMARY

This paper presents on-chip characterization of electrostatic discharge (ESD) impacts applied on the Si-substrate backside of a flip-chip mounted integrated circuit (FC-IC) chip. An FC-IC chip has an open backside and there is a threat of reliability problems and malfunctions caused by the backside ESD. We prepared a test FC-IC chip and measured Si-substrate voltage fluctuations on its frontside by an on-chip monitor. The voltage surges as large as 200 mV were observed on Si-substrate voltage fluctuations on its frontside caused by the backside ESD. We prepared a test FC-IC chip and measured backside and there is a threat of reliability problems and malfunctions among thinned Si substrates up to 40 µm, and also explained in full-system level simulation of backside ESD impacts with the equivalent models of ESD-gun operation and FC-IC chip assembly.

key words: Electrostatic discharge, Full-wave simulation, On-chip monitor, Flip-chip assembly, Integrated circuit.

1. Introduction

The tolerance of semiconductor integrated circuit (IC) chips to high power transient disturbances in the surrounding environment is extremely important. With respect to failure modes, there are permanent and temporary failures. Although temporary failures are recovered by turning the power back on, this remains problematic for reliability in the applications such as automotive and medical healthcare which rely on real-time performance (Figure 1). Generally, IC chips are verified to have a certain level of immunity to external disturbances such as electromagnetic field irradiation and conductive radio frequency (RF) power injection following to semiconductor electromagnetic compatibility (EMC) test standards [1]-[3]. The magnitude and frequency of RF disturbances are investigated to determine the threshold at which an IC chip may malfunction, and to verify compliance with EMC regulations that are set forth in the respective field of application. In addition, IC chips must also withstand electrostatic discharge (ESD), which is an instantaneous high voltage surge [4]. ESD protection is very important and its evaluation methods have been discussed [5]-[8]. ESD guns emulate ESD waveforms to reproduce real-world ESD discharges, as mimicking the instantaneous discharge of electrical charges on humans and devices, causing high-voltage fluctuations to the device under test (DUT) system. In ESD measurement, it is difficult to precisely determine the current paths in the DUT, while a pass or fail evaluation can be conducted. ESD gun models have been proposed for ESD standards at the simulation level [9]-[11], and full-wave 3D electromagnetic field simulation has been conducted for a PCB-level ESD analysis method [12]-[14]. A method for observing ESD waveforms when ESD enters through the input/output (I/O) pins of ICs has also been devised [15]. However, since the susceptibility of IC chips to transient disturbances except for I/O pins is affected by the structure and materials of the package, the analysis of ESD paths due to differences in IC chip structure remains challenging. IC chips are equipped with many I/O pins for high functionality, and flip-chip mounting has become general practice due to the demand for smaller sizes and lower profiles. Consequently, the backside of IC chips is an open surface that is susceptible to transient disturbances, either spontaneous or intentionally applied. This has emerged as a new reliability issue in safety-critical IC chips and related electronic devices.

From another perspective, security concerns exist. The attempts to analyze cryptographic key information by intentionally causing a fault by a malicious attacker have been reported [16]. Attack methods include voltage, electromagnetic waves, lasers, and heat, each of which has its own characteristics such as locality, timing control, and cost [17]-[21]. Backside voltage pulse attacks on flipped chips have been discussed and models for generating temporary faults have been proposed [22]. However, the observation of the disturbance has not been realized due to measurement difficulties, and accurate characterization has not yet been achieved.

In this paper, a prototype flip-chip mounted integrated circuit (FC-IC) chip was prepared in a 0.13 µm CMOS process. High-voltage pulse applied on the IC-chip backside propagates through the silicon substrate and reaches CMOS ICs on the frontside. The voltage peaks are evaluated with an on-chip voltage monitor. The variation of the characteristics of the propagation path depending on the thickness of the silicon substrate will also be discussed. Furthermore, a coupled simulation method of the silicon chip model using an ESD gun model and a 3D simulation is devised.
The remainder of this paper is organized as follows. Section 2 presents the concept of ESD impacts from the backside of IC chips in flip chip mounting and compares it with existing test standards. Sections 3 and 4 provide an overview and results of Backside ESD measurements and simulations, respectively. Finally, Section 5 provides a brief summary of the findings.

2. Backside ESD Impacts

Figure 2 explains the backside ESD and highlights the differences from standard ESD test methods, with comparisons to existing ESD standards (Table 1). Typically, an ESD evaluation uses a high-voltage disturbance to a single pin of interest on an IC chip. The DUT is tested under the conditions where ESD current is absorbed and mitigated into the power supply network via ESD protection diodes in the pin I/O cells around the die. The impacts are given through transmission line pulsing (TLP) in the human body model (HBM), zapping in the charge device model (CDM) stress, and stressing by an ESD gun for a system level stress, and so forth [23], [24]. The protection performance criteria for IC chips include self-healing where any function is not lost, and the tolerance in which no change occurs in the actual operating state or among the stored data [25], [26]. One of I/O pins is chosen as the contact point for ESD testing and checked for those criteria. This is repeated one after another among the I/O pins.

Backside ESD, on the other hand, allows a more straightforward application of high voltage impacts without concern about the placement of circuitry on the front side. FC ICs may not be molded for heat dissipation structure. If the IC chip is molded, it will be chemically or mechanically treated to create holes on the plastic laminate. This process eliminates the permanent breakdown, unlike face-up mounted ICs, there is no need to worry about damaging wires or surface circuits.

If a high voltage is applied to the backside resin or the Si-substrate backside of an IC chip, the ground (or drilled) resin and silicon substrate act as "resistance" and induce a voltage surge that reaches the circuitry on the front side. This reaches the internal circuitry directly, almost independently of the ESD protection diodes on the front side. This can cause the internal bits of the logic data register to invert unexpectedly, resulting in erroneous outputs or even malfunction of entire circuitry.

Table 1 compares the parameters of our backside ESD experiment with those of conventional ESD standards. The output voltage is provided by a lower than the conventional ESD standard, and the tip of the ESD gun is selected to be the contact type for measurement repeatability. The voltage variations associated with this ESD impact are observed on the surface side by the on-chip monitor circuitry described below. As mobile devices become smaller and lower-profile, flip-chip mounting of IC chips has become the mainstream, and backside laminates are becoming thinner than ever. In addition, these trends motivate and facilitate malicious attempts by adversaries to intentionally grind or drill the backside resin to inject defects for side-channel attacks [27]-[29].

3. Backside ESD Experiments

3.1 Prototype chip

The backside ESD is evaluated with the prototype FC IC chip given in Fig. 3. To characterize the backside ESD, Si substrates of the IC chip were thinned down with the thicknesses of 350 \( \mu \)m, 150 \( \mu \)m, and 40 \( \mu \)m, as shown in Fig. 4.

The on-chip voltage monitor (OCM) circuit (Figure 5) captures the voltage waveforms at the probing points. A total of 20 points are located along concentric circuits in the center of the chip, and contacted to p+ contact diffusions on the p-type Si substrate. The OCM consists of an input buffer and an analog-to-digital converter (ADC) and outputs the voltage data to the off-chip in digital codes. The input buffer uses a source follower circuit to drive the signal over a wide
bandwidth [30]. Though the voltage level on the target substrate is near \( V_{SS} \), the p-MOS source follower shifts the DC level into the input range of the ADC. The OCM is isolated from other circuits by a triple-well structure, and measures the small changes in the substrate voltage. Here, the supply voltage at the OCM is 1.8 V, and the maximum input voltage \( V_{max} \) to the p-MOS source follower is safely designed as approximately 1.0 V.

3.2 Experimental setup

The ESD gun shown in Figure 6 discharges when triggered and generates high-voltage pulses as current flows through the contact resistance of the \( R_{CON} \) and the contact needle in series with the ohmic contact from its backside to the Si substrate. The parameters of the RC module of the ESD gun are 2 k\( \Omega \) for the resistance and 330 pF for the capacitor, according to one of the standard specifications. The \( R_{CON} \) simulates a thin plastic laminate on the backside of the chip, representing the series resistance between the ESD contact point and the silicon substrate. The current will be spatially distributed throughout the Si substrate, inducing the position dependence on the voltage surge. Photographs of the experimental setup are also shown. The contact needle is fine enough (approximately 170 \( \mu m \) in diameter) to scan the backside of the IC chip, and if the chip contains functional circuits or systems, the micro-movements allow the investigation of circuit-level sensitivity to voltage surges. The discharge voltage of the ESD gun is defined as \( V_{ESD} \).

3.3 Experimental result

The voltage surge waveforms measured by the OCM are shown in Fig. 7 when the backside ESD impact is applied to the center of the FC-IC chip, for different contact resistance \( (R_{CON} = 5k, 100k, 1\text{Meg} \Omega) \) and silicon thickness \( (H = 350, 150, 40 \mu m) \). It is noted that the measurable range is limited by the OCM, and results may not be obtained under extreme conditions.

The peak-to-peak voltage \( V_{peak} \) is clearly dependent on the relative distance between the needle attachment point on the backside and the monitoring probe on the frontside, as shown in Figure 7. The distance \( L \) is calculated from the
Fig. 7  ESD waveform at 200V measured by the on-chip monitor [31].

The maximum $V_{\text{peak}}$ was 200 mV for a conventional Si thickness of 350 µm with $R_{\text{CON}}$ of 5 kΩ and a discharge voltage of 200 V when the needle and probe were at approximately the same position. On the other hand, when the die is thinned down to 40 µm, $V_{\text{peak}}$ increases to 15mV at the same position with 1 Meg Ω, and increases with smaller $R_{\text{CON}}$, indicating that the back surface resin is further scraped off. These voltage values can be compared to the potential. $V_{\text{peak}}$ is expected to be higher than $V_{\text{max}}$ at 40 µm and 5 kΩ in the matrix of Fig. 7, so it is shown only for simulation (see Sect. IV).

4. Backside ESD simulation

4.1 Simulation setup

The conceptual diagram in Figure 8 depicts our framework for simulating the voltage spikes on a chip produced by the backside ESD. The framework provides equivalent circuit models for integrated circuit simulation for an ESD gun and an IC chip Si substrate in "sp" files, respectively.

The charging and discharging mechanism of an ESD gun is represented by a switch matrix. The instantaneous current is characterized by the RC module $(R_c, C_c)$ defined by the standard and the parasitic inductance $(L_s, L_c)$ and parasitic capacitance $(C_t)$ due to the gun tip and return ground cable. These passive components are fitted by capturing the ESD voltage waveforms generated on a standard load resistor ($R_{\text{load}} = 50$ Ω) with an oscilloscope. Figure 9 shows a comparison of measured and simulated ESD gun output waveforms, with the first peak and transient response coinciding.

As shown in Figure 10, we placed explicit electrical ports on the Si substrate model, with the injection contacts on the back side and the locations probed by OCM and the connections to $V_{\text{SS}}$ of the I/O cells on the front side. A full-wave electromagnetic solver was used to extract the corresponding S-parameters between each port, and the model was dropped into a multi-node equivalent circuit in the form of an RC network. The parameters in the simulation are listed in Table 2.
A circuit simulator is applied to the netlist integrating ESD gun and Si substrate sub-models to generate waveforms.

4.2 Simulation and validation

Figure 11 gives the comparison of measurements and simulation of the backside-ESD results on FC-IC chip for $V_{\text{peak}}$ when $V_{\text{ESD}}$ is 200 V. The measurements are made for a total of 20 points of OCM probes spread concentric circles as shown in Fig. 3. Regarding the simulation, the OCM port is placed in the same position as the prototype chip. When $V_{\text{peak}}$ was drawn against the spatial distance ($L$) between the injection needle contact point and the OCM probe point, the measured and simulated trends were almost the same under different $H$ and $R_{\text{CON}}$ conditions. The results show that the integrated circuit simulation of the respective equivalent circuits of the ESD gun and the IC chip Si substrate works well.

Figure 12 shows that $V_{\text{peak}}$ decreases proportionally to the increase of $R_{\text{CON}}$ as measured at the OCM probe point located closest to the injection point. With the silicon thickness of 40 µm, the mold resin is reproduced by the $R_{\text{CON}}$ of 1 MegΩ, and $V_{\text{peak}}$ becomes 30 mV at a discharge voltage of 600 V. We have observed in [15] that voltage fluctuations as large as 200 mV can invert the logic values of flip-flop-based data registers. Simulations show that when the silicon substrate is thinned to 40 µm, voltage fluctuations of 200 mV occur on the front side when $V_{\text{ESD}}$ and $R_{\text{CON}}$ are 3kV and 1MegΩ, respectively. This suggests that backside ESD may affect the circuit operation on the front side.

In addition, Figure 13 analyzes a heat map of the frontside $V_{\text{peak}}$. In the left graph, the highest $V_{\text{peak}}$ is naturally found at the center of the ESD, which is approximately at the same coordinates as the ESD contact point. On the other hand, the right graph plots the attenuation ratio from the highest $V_{\text{peak}}$, and the spread of $V_{\text{peak}}$ becomes wider for the thicker Si substrates. This is obviously to be expected from the spherical expansion of voltage surges. These trends validate the simulation framework. Furthermore, we observe that when Si substrate becomes thinner, the localization of backside ESD becomes more pronounced, and there is a risk of malicious and intentional backside search contributing to the occurrence of fault injection.

<table>
<thead>
<tr>
<th>Model</th>
<th>Frequency sweeps</th>
</tr>
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<tbody>
<tr>
<td>RC module</td>
<td>2 kΩ, 330 pF</td>
</tr>
<tr>
<td>Si resistivity</td>
<td>0.01 Ω·m</td>
</tr>
<tr>
<td>Si thickness</td>
<td>350, 150, 40 µm</td>
</tr>
</tbody>
</table>
Fig. 11  $V_{\text{peak}}$ at 200 V in measurement and simulation [31].

Fig. 12 Comparison of $V_{\text{peak}}$ between measurement and simulation [31].
Fig. 13 The heatmaps of the frontside $V_{\text{peak}}$ [31].

5. Conclusion

The backside ESD impacts on FC-IC chips were evaluated by on-chip monitoring in prototype chips for voltage surges and full stack simulation. The voltage distribution on the silicon substrate in the surface circuit in FC-BGA ICs was observed. For backside ESD impacts, the voltage fluctuation amplitude generated in the surface circuit depends on parameters such as the thickness of the silicon substrate. It was suggested that the thinner the silicon chip, the higher the threat of localized exposure.

Among the sources of disturbance, the backside ESD generates voltage fluctuations on the front side more efficiently with simple measurement setups. This can be utilized as an experimental platform to develop semiconductor IC chips that are highly reliable and tolerant to environmental disturbances.

The simulation framework for backside ESD, which is different from conventional ESD intrusion from I/O pins, was established by modeling IC chips using 3D electromagnetic field simulation and by co-simulating with an ESD gun model. Further considerations will be conducted by combining transistor-level circuit models to simulate the interaction between the induced voltage surges and circuit operation.

References


Takuya Wadatsumi received the B.S. and M.S. degrees in engineering from Kobe University, Kobe, Japan, in 2019 and 2021, respectively, where he is currently pursuing the Ph.D. degree in the fields of hardware security and electromagnetic compatibility.

Kohei Kawai received the B.S. degree in engineering from Kobe University, Kobe, Japan, in 2021, where he is currently pursuing the M.S. degree in the field of electromagnetic compatibility.
Rikuu Hasegawa received the B.S. degree in engineering from Kobe University, Kobe, Japan, in 2022, where he is currently pursuing the M.S. degree in the field of hardware security.

Kikuo Muramatsu received ~

Hiromu Hasegawa received the B.S. degree in engineering from Kyoto University, Kyoto, Japan, in 1990, after joined Mitsubishi Electric Corp. in 1990, and Minolta Co., Ltd in 1998, is currently working for MegaChips Corp. since 2002.

Takuya Sawada received a B.E. and M.E. degree in Department of Computer and System Engineering, Faculty of Engineering, Kobe University in 2008 and 2010, respectively, and received a Ph.D. degree in Graduate School of System Informatics, Kobe University in 2013. He currently works as a semiconductor chip designer at MegaChips Corporation, Osaka, Japan.

Takahito Fukushima received the B.S. degree in material engineering from Tokyo University of Science, Tokyo, Japan, in 1992. From 1992 to 2022, he was an engineer of development of semiconductor products at Megachips Corporation, Japan, and was also researching Electromagnetic compatibility of communication device related to automotive products.

Hisashi Kondo received the B.S. and M.S. degrees in electrical engineering from Kyoto University, Kyoto, Japan, in 1985 and 1987, respectively. After working for multiple companies in the semiconductor industry, now he is the independent consultant in this field.

Takju Miki received the Ph.D. degree from Kobe University, Kobe, Japan, in 2017. From 2006 to 2016, he was with Panasonic Corporation, Osaka, Japan, where he was involved in the development of analog and mixed-signal integrated circuits for consumer and industrial applications. He is currently an Associate Professor with the graduate school of science, technology and innovation, Kobe University. His current research interests include data converters, hardware security and cryogenic CMOS circuits for quantum computers.

Dr. Miki is currently serving as a member of technical program committees for the IEEE Asian Solid-State Circuits Conference and the IEEE European Solid-State Circuits Conference. He has served as a Guest Editor for special section on analog circuits and their application technologies of IEICE Transactions on Electronics since 2022.

Makoto Nagata received the B.S. and M.S. degrees in physics from Gakushuin University, Tokyo, Japan, in 1991 and 1993, respectively, and the Ph.D. degree in electronics engineering from Hiroshima University, Hiroshima, Japan, in 2001. He was a Research Associate at Hiroshima University from 1994 to 2002, an Associate Professor at Kobe University, Kobe, Japan, from 2002 to 2009, where he was promoted to a Full Professor in 2009. He is currently a Professor with the Graduate School of Science, Technology and Innovation, Kobe University. His research interests include design techniques targeting high-performance mixed analog, RF and digital VLSI systems with particular emphasis on power/signal/substrate integrity and electromagnetic compatibility, testing and diagnosis, three-dimensional system integration, as well as their applications for hardware security and safety.