SUMMARY In this paper, we propose a hybrid crystal oscillator which achieves both quick startup and low steady-state power consumption. At startup, a large negative resistance is realized by configuring a Pierce oscillating circuit with a multi-stage inverter amplifier, resulting in high-speed startup. During steady-state oscillation, the oscillator is reconfigured as a class-C complementary Colpitts circuit for low power consumption and low phase noise. Prototype chips were fabricated in 65nm CMOS process technology. With Pierce-type configuration, the measured startup time and startup energy of the oscillator are reduced to 1/11 and 1/5, respectively, compared with the one without Pierce-type configuration. The power consumption during steady oscillation is 30 μW.

key words: Crystal oscillator, quick startup, low power, low phase noise, class-C, Complementary Colpitts

1. Introduction

Crystal oscillators are employed in various electronic devices, such as wireless circuits and microcontrollers, to generate a reference clock with high frequency accuracy. For IoT applications, these devices are demanded to operate with ultralow power consumption. A crystal oscillator in an IoT device achieves ultralow power consumption through duty cycling, i.e. it operates only when wireless communication or signal processing is carried out [1]. Fig. 1 shows the circuit topology of a conventional Pierce crystal oscillator and the equation of its startup time [2], [3]. In a general MHz-band crystal oscillator, the quality factor of the crystal is high, ranging from tens of thousands to hundreds of thousands, resulting in startup time of hundreds of μs to several ms. Since the generated reference clock is not available during this period, the energy consumed by the crystal oscillator and other circuits is wasted. To solve this issue, several methods have been proposed to shorten the startup time of a crystal oscillator [4]. Generally, there are three methods: in [5]-[11], the negative resistance |Rn| of the oscillating circuit is increased; in [12]-[22] the initial current |I0(0)| is exaggerated by injecting frequency components near the oscillation frequency; in [23]-[25], the load capacitance CT decreased. These techniques have successfully reduced the startup energy down to several tenths. On the other hand, low power consumption during steady-state oscillation is also important for IoT devices. We have proposed a complementary Colpitts oscillating circuit that operates in class-C, successfully achieving low power consumption and low phase noise [26], [27]. However, when the oscillator is transitioning to class-C operation, the negative resistance decreases as the reduced current of the source follower, leading to a longer startup time. While a booster circuit using a pseudo-random signal is employed in [26] to shorten the startup time, we believe further improvement of startup acceleration is possible.

In this paper, we propose a hybrid crystal oscillator that achieves both quick startup and low steady-state power consumption. At startup, a large negative resistance is realized by configuring a Pierce oscillating circuit with a multi-stage inverter amplifier, resulting in high-speed startup. During steady-state oscillation, the oscillator is reconfigured as a class-C complementary Colpitts circuit for low power consumption and low phase noise. This paper is organized as follows. Section 2 presents the basic configuration of a hybrid crystal oscillator and describes each mode of operation. In Section 3, we analyze the effect of the frequency deviation caused by switching the operating mode, and the effect on the performance due to the switch on-resistance. Section 4 summarizes the measurement results of the prototype crystal oscillator. Section 5 draws the conclusion.
2. Proposed Hybrid Crystal Oscillator

2.1 Basic concept of proposed oscillator

Figure 2 shows a basic configuration of the proposed hybrid crystal oscillator (Hybrid XO in the following context). Figure 2(a) shows the basic topology. It consists of one crystal oscillator $X_1$, three capacitors $C_1$ to $C_3$, switches $S_1$ for switching the configuration of the oscillation circuit, an inverter with an enable function, and a source follower circuit. Bias circuits for each amplifier are omitted for simplicity of explanation.

Figure 2(b) shows the configuration of the Pierce oscillation circuit mode (Pierce XO mode). For the Pierce type, $S_1$ is turned OFF. Also, the inverter is enabled, and the source follower is disabled. Although $C_2$ and $C_3$ are connected in series, this is a generic Pierce-type oscillator. Such a Pierce oscillator is widely used because it has a simple topology and can meet the oscillation conditions relatively easily. In addition, various methods have been proposed to speed up the startup [5] - [25]; they are possible to be employed as well.

Figure 2(c) shows the configuration of the Colpitts oscillator mode (Colpitts XO mode). For this configuration, $S_1$ is turned ON. Also, the inverter is disabled, and the source follower is enabled. A Colpitts oscillator is known to have low phase noise from the viewpoint of the oscillator impulse sensitivity function (ISF) [28], promising to high power efficiency. Hence, the proposed hybrid topology, embracing the merits of the Pierce and Colpitts oscillators is expected to achieve both quick startup and ultralow steady-state power consumption.

2.3 Circuit Implementation

Figure 3 shows the detailed circuit configuration of each oscillation mode and the startup sequence. For simplicity of explanation, $S_1$ in Fig. 2 is omitted in each figure.

The Pierce XO mode adopts the multi-stage amplifier proposed in [6], as shown in Fig. 3(a). It consists of three stages of inverters, and the transconductance of the inverter in the third stage is equivalently increased by the voltage amplifiers in the first and second stages. In addition, owing to the phase rotation by $C_T$, the negative resistance near the oscillation frequency of the crystal oscillator is increased beyond the theoretical limit of the conventional circuit [6].

In the Colpitts XO mode, as shown in Fig. 3(b), low power consumption and low phase noise are achieved by using a complementary Colpitts operating in class-C [26].

From the respective measurement results, the configuration in Fig. 3(a) has excellent startup characteristics, but the power consumption in the steady state is high. On the other hand, though the configuration shown in Fig. 3(b) has slow startup characteristics, the oscillator features low steady-state power consumption and low phase noise.

To take all the advantages while compensating for the drawbacks of each, as shown in Fig. 3(c), Pierce XO mode is used at startup and Colpitts XO mode is used at steady state. Since the negative resistance is high in the Pierce XO mode at startup, the oscillation amplitude grows quickly, and the energy of the oscillation frequency component is stored in the crystal unit as vibrational energy. When the oscillation amplitude becomes sufficiently large, the oscillator is switched from Pierce XO mode to Colpitts XO mode. As shown in Fig. 3(b), before mode switching, the gate voltages of the source follower NMOS and PMOS are connected to $V_{DD}$ and $V_{SS}$, respectively. This results in the maximum bias current once the source follower is enabled. Therefore, the voltage of $V_{XO2}$ quickly settles to a steady-state voltage and functions as an oscillation circuit without interruption. Roughly estimating the settling time $t_{set}$ for $V_{XO2}$, $t_{set} = C_3 V_{set}/I_b = 60$ ns, assuming $C_3 = 12pF$, bias current $I_b = 100\mu A$, and the steady-state voltage $V_{set} = 0.5V$. The quality factor (Q) of a crystal oscillator is high, so the vibrational energy does not attenuate immediately [29], [30]. Since the mode switching time is sufficiently short compared to the damping time of vibration energy (hundreds of μs to several ms for oscillators in the MHz band), it is possible to switch while the oscillation continues. Hence, a large oscillation amplitude ready right after the oscillator enters Colpitts XO mode, which leads to an immediate available reference clock.

Figure 4 shows the transient simulation results of Hybrid XO and using Cadence Spectre. Table 1 shows the parameters of the crystal unit whose oscillating frequency is 32 MHz (according to the equivalent circuit in Fig. 1) and
capacitors (according to Fig. 2) used in the simulation. Assuming that the load capacitance of the oscillator is $C_{L_P}$ in Pierce XO mode and $C_{L_C}$ in Colpitts XO mode, using the circuit variables in Fig. 3,

\[ C_S = 2C_C + \frac{C_2C_3}{C_2 + C_3} \]  
\[ C_{L_P} = \frac{C_1C_S}{C_1 + C_S} \]  
\[ C_{L_C} = \frac{C_2C_3}{C_2 + C_3} \]

are derived. The oscillation frequency $f$ of the crystal oscillator is [2],[3]

\[ f = f_r \left( 1 + \frac{C_M}{2(C_P + C_L)} \right) \]

where $f_r$ is the resonant frequency of the crystal and $C_L$ is the load capacitance of the oscillator. From these equations and parameters in Table 1, $C_{L_P}$ and $C_{L_C}$ are 6pF, resulting in equal oscillation frequencies in each mode is expected.

The oscillating circuit is simulated in 65-nm CMOS process with 1.0-V power supply. In this simulation, the Hybrid XO switches to Pierce XO mode after 10 ns and to Colpitts XO mode after 60μs. Fig. 4(a) shows the output voltage of each oscillator. The signal amplitude grows quickly in Pierce XO mode, and a sufficient signal amplitude is obtained immediately after switching. The time until the amplitude reaches 90% of maximum amplitude is about 1150μs when starting with only Colpitts XO, while it is 60μs with Hybrid XO, which is 19 times faster. Fig. 4(b) shows the current consumption of each oscillator. The average current...
Table 1 Circuit parameters for simulation in Fig.4.

<table>
<thead>
<tr>
<th>Crystal unit</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_m$</td>
<td>15.3Ω</td>
</tr>
<tr>
<td>$L_m$</td>
<td>6.68mH</td>
</tr>
<tr>
<td>$C_m$</td>
<td>3.7fF</td>
</tr>
<tr>
<td>$C_p$</td>
<td>1.4pF</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Capacitors</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_1$</td>
<td>9pF</td>
</tr>
<tr>
<td>$C_2$</td>
<td>12pF</td>
</tr>
<tr>
<td>$C_3$</td>
<td>12pF</td>
</tr>
<tr>
<td>$C_C$</td>
<td>6pF</td>
</tr>
</tbody>
</table>

consumption of Hybrid XO mode is 204 μA, which is larger than Colpitts XO’s 110 μA. However, when comparing the energy required for startup, the Hybrid XO consumes 12.2 nJ while the Colpitts XO consumes 127 nJ. The former is about 1/10 of the latter due to the shortened startup time. As for the power consumption during steady-state oscillation, the average value is kept as low as 28 μA owing to the Complementary Colpitts class-C operation. Thereby, both high-speed startup, low energy consumption and low steady-state power consumption are expected to be achieved.

3. Design Consideration of Hybrid Crystal Oscillator

3.1 Design Considerations

The performance of the proposed Hybrid XO is mainly determined by the Pierce XO and the Colpitts XO, and most features of both can be achieved. However, the Hybrid XO configuration presents two new design challenges. First, the frequency settling time when switching the modes must be considered. If the oscillation frequencies are different between the Pierce XO mode and the Colpitts XO mode, it may take time for the frequency to settle to the desired value after mode switching. Second, the on-resistance of the switches for changing the configuration can affect the circuit performance. In particular, the effects on phase noise and power consumption during steady-state oscillation must be considered. This chapter analyzes these issues.

3.2 Oscillation Frequency Settling time

In this paper, since Pierce XO is used at startup and Colpitts XO is used during steady-state oscillation, the fluctuation of the oscillation frequency of Colpitts XO after mode switching is considered. The amount of frequency change $\Delta f_0/f$ as the difference of the load capacitance $\Delta C_L = C_{L,C} - C_{L,P}$ is derived from equation (4) as follows.

$$\frac{\Delta f_0}{f} = -\frac{c_m}{2(c_f+c_L)^2}\Delta C_L$$  \hspace{1cm} (5)

Because external chip capacitors can be used for $C_1$, $C_2$, and $C_3$, the capacitance variation is generally less than 1%.

On the other hand, since $C_C$s are implemented in integrated circuits, they are affected by process variations. As a result, absolute capacitance variations of $+/-20~30\%$, which is the main cause of $\Delta C$. Figure 5 shows the transient simulation results of the frequency settling after mode switching for the Hybrid XO described in section 2.3, when $C_C$ varies from 4 pF to 8 pF (6 pF $+/-$33%). In this simulation, Pierce XO mode is enabled and then switched to Colpitts XO mode 100 μs later. The frequency deviation $\Delta f_0/f$ is calculated with respect to the oscillation frequency of the stable state in case of $C_C = 6$ pF. A large frequency fluctuation is observed immediately after switching, but this is caused by the shift of the DC operating point of the source follower due to the mode switching. A smaller $C_C$ results in a faster return to the DC operating point and shorter frequency settling time, but there is a tradeoff with phase noise, which must be carefully determined. Even including this variation, the frequency settling time within $+/-20$ ppm is less than 5 μs, which is sufficiently short compared to the amplitude start time, as shown in Fig. 6. Therefore, even if there is a certain amount of error between the frequency at startup and the oscillation frequency at the steady state, it can be expected that the effect on the startup time is minor. Basically, it is desirable to match $C_{L,P}$ and $C_{L,C}$ within a certain range so that they are within the allowable value of the frequency deviation that can be obtained from equation (5).
3.3 Influence of Switch On-resistance

Since the configuration shown in Fig. 2(c) is used during steady-state oscillation, it is affected by the on-resistance of switch $S_1$. This on-resistance is inserted in series with the crystal oscillator; thus, a large resistance suppresses oscillation amplitude and degrades phase noise. Also, the resistive loss can affect the power consumption of the oscillator. This section addresses these concerns.

Figure 7(a) shows the simulated phase noises when the on-resistance of $S_1$ is varied from 1 $\Omega$ to 100 $\Omega$. As the resistance increases, the overall phase noise increases. Fig. 7(b) shows the phase noise at 1-kHz offset with different on-resistance. For example, to suppress the increase of the phase noise to 3 dBc/Hz or less, it is necessary to reduce the on-resistance of the switch to approximately 20 $\Omega$ or less. Fig. 8 shows the relationship between the steady-state current consumption of the Colpitts oscillator and the on-resistance of switch $S_1$. It becomes necessary to generate a negative resistance in the oscillation circuit to cancel the loss due to the on-resistance of the switch. The negative resistance of the oscillating circuit is proportional to the transconductance of the source follower, according to the negative resistance equation shown in Fig. 1. Also, since the transconductance is proportional to the average bias current of the source follower, as a result, the current consumption increases almost proportionally to the increase of the on-resistance. With the above considerations, since the on-resistance of switch $S_1$ leads to increased phase noise and current consumption, it must be kept as low as possible. Since the switch of $S_1$ is connected to $V_{SS}$, an NMOS transistor can be used as a switch, and the voltage between the gate and the source can be applied to $V_{DD}$. Thus, low resistance can be implemented relatively easily. In this design, the NMOS switch size of $S_1$ is determined so that the on-resistance of the switch is about 1 $\Omega$. 

### Table 2 Crystal unit parameters for the measurement.

<table>
<thead>
<tr>
<th>Crystal unit</th>
<th>$R_M$</th>
<th>$L_M$</th>
<th>$C_M$</th>
<th>$C_P$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_M$</td>
<td>21.6 $\Omega$</td>
<td>$L_M$</td>
<td>5.82 mH</td>
<td>4.25 fF</td>
</tr>
<tr>
<td>$L_M$</td>
<td>$C_M$</td>
<td>0.94 pF</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$C_M$</td>
<td>$C_P$</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

![Chip photo of proposed hybrid XO.](image)

![Simulation result of phase noise. Switch on resistance of $S_1$ is from 1$\Omega$ to 100$\Omega$.](image)

![The switch on resistance vs. phase noise at 1kHz offset frequency.](image)

![The switch on resistance vs. current consumption of Colpitts oscillator at steady state.](image)
4. Measurement Results

Prototype chips of the proposed Hybrid XO were fabricated in 65-nm CMOS technology. Fig. 9 shows the chip photo. The chip area is 0.031mm².

Table 2 shows the parameters of the crystal unit for evaluation. The oscillation frequency is 32 MHz, and the load capacitances $C_{L,P}$ and $C_{L,C}$ of the oscillator are designed to be 9 pF. In subsequent measurements, the power supply voltage is 1.2V. Fig. 10 shows the measured startup waveforms of the oscillator. In Fig. 10(a), Colpitts XO mode from startup to steady state is shown. The measured amplitude startup time which reaches 90% of maximum amplitude is 1270 μs. Fig. 10(b) shows Pierce XO mode for 110 μs at the startup. Then, the oscillator was switched to Colpitts XO mode. The amplitude startup time is 110 μs, i.e., 11.5-time improvement. Fig. 11 shows the relationship between the time until the oscillation frequency settles within ±10 ppm of the steady state and the period of the Pierce XO mode. The amplitude startup time is 1468 μs when Pierce XO mode is not configured, while it becomes 127 μs when Pierce XO mode is turned on for a period of 110 μs. Similar to the amplitude startup time, 11.5 times of improvement is achieved. Also, since the 10% difference between the amplitude startup time and the frequency startup time is not so large, the former is used as the startup time in the following results.

Fig. 12(a) shows stability of the steady-state oscillation frequency with varied temperatures. The frequency deviation is within ±10 ppm (25°C reference) in the range of -40°C to 85°C. Thus, the oscillation frequency is as stable as the one of a normal crystal oscillator. Fig. 12(b) shows the startup time at different temperatures. When Pierce XO mode is not used, the startup time fluctuates by about 450 μs.
Table 3 Performance summary and comparison.

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology Node (nm)</td>
<td>65</td>
<td>65</td>
<td>65</td>
<td>65</td>
<td>22</td>
<td>65</td>
</tr>
<tr>
<td>Supply (V)</td>
<td>1.2</td>
<td>1.2</td>
<td>1</td>
<td>1.2</td>
<td>-</td>
<td>1.2</td>
</tr>
<tr>
<td>Frequency (MHz)</td>
<td>32</td>
<td>40</td>
<td>24</td>
<td>20</td>
<td>38.4</td>
<td>32</td>
</tr>
<tr>
<td>Load capacitance (pf)</td>
<td>9</td>
<td>9</td>
<td>6</td>
<td>4</td>
<td>15.4</td>
<td>6</td>
</tr>
<tr>
<td>Active area (mm²)</td>
<td>0.0031</td>
<td>0.0053</td>
<td>0.012</td>
<td>0.046</td>
<td>0.07</td>
<td>(w/o LDO)</td>
</tr>
<tr>
<td>Startup time (µs)</td>
<td>127.1 (+10ppm)</td>
<td>64.1 (+40ppm)</td>
<td>1100</td>
<td>30</td>
<td>50</td>
<td>7.2 (+20ppm)</td>
</tr>
<tr>
<td>Startup energy (nJ)</td>
<td>65.3</td>
<td>37.2</td>
<td>125</td>
<td>11.1</td>
<td>39.4</td>
<td>3.6</td>
</tr>
<tr>
<td>Steady state power consumption (µW)</td>
<td>30</td>
<td>141</td>
<td>19</td>
<td>169</td>
<td>696</td>
<td>(w/ LDO) 70</td>
</tr>
<tr>
<td>Quick startup technique</td>
<td>NRB</td>
<td>NRB</td>
<td>DI</td>
<td>NRB=DI</td>
<td>NRB+CI</td>
<td>Si+SC</td>
</tr>
</tbody>
</table>

NRB: Negative Resistance Boosting, DI: Dither Injection, CI: Chirp Injection
SI: Self-timed Injection, SC: Stepwise Charging

in the range of -40°C to 85°C. When using Pierce XO mode for 110 µs at startup, a stable startup time is achieved.

Table 3 summarizes the performance of the Hybrid XO and the performance comparison of other papers. It is notable that the proposed crystal oscillator has the merits of both VLSI ’18 and SSCL ’20. In addition, the energy reduction effect is competitive with other papers.

5. Conclusion

This paper proposed a hybrid XO that combines the advantages of Pierce XO and Colpitts XO. We applied negative resistance boost technology to the Pierce XO for quick startup. The complementary Colpitts XO operates in class-C, achieving low power consumption in steady state. Although there are concerns of the increase of frequency settling time due to frequency deviation during mode switching, and the degradation of phase noise as well as power consumption due to switch on-resistance. The simulations suggest minor influence on the oscillator’s performance. Prototype chips in 65-nm CMOS were evaluated. The results suggest 11 times of faster startup owing to Pierce XO, and the startup energy reducing to 1/5. In addition, it was confirmed that the power consumption of the Colpitts XO is as low as 30 µW in the steady state.

Acknowledgments

This work was supported by World Premier International Research Center Initiative (WPI), MEXT, Japan. The EDA tools for this paper are provided through the activities of d.lab, the University of Tokyo in collaboration with Cadence Design Systems, Inc. and Mentor Graphics, Inc.

References

400


[29] S. Iguchi, A. Saito, Y. Zheng, K. Watanabe, T. Sakurai and M. Takamiya, "93% power reduction by automatic self power gating (ASPG) and multistage inverter for negative resistance (MINR) in 0.7V, 9.2μW, 39MHz crystal oscillator," 2013 Symposium on VLSI Circuits, 2013, pp. C142-C143.


Masaya Miyahara received B.E. degree in Mechanical & Electrical Engineering from Kisanaru National College of Technology, Kisanaru, Japan, in 2004, and M.E. and Ph.D. degree in Physical Electronics from Tokyo Institute of Technology, Tokyo, Japan, in 2006 and 2009 respectively. From 2009 to 2017, he was an Assistant Professor at Department of Physical Electronics, Tokyo Institute of Technology, Tokyo, Japan. He has been an Associate professor at Institute of Particle and Nuclear Studies (IPNS) since 2017, and a Principal Investigator at International Center for Quantum-field Measurement Systems for Studies of the Universe and Particles (QUPI) since 2021, in High Energy Accelerator Research Organization (KEK), Ibaraki, Japan. His research interests are Mixed signal circuits and Sensor read-out LSI for particle and nuclear physics experiments. He is a member of IEEE Solid-State Circuits Society and The Institute of Electronics, Information and Communication Engineers (IEICE). He is/was a member of the technical program committees of A-SSCC and Associate Editor of IEICE Transaction on Electronics.

Zule Xu received the B.E. degree in Electrical Engineering from Dalian University of Technology, Dalian, China, in 2006, the M.E. degree in Electrical Communication Engineering from Tohoku University, Sendai, Japan, in 2011, and the Ph.D degree in Physical Electronics Engineering from Tokyo Institute of Technology, Tokyo, Japan, in 2015. From 2015 to 2016, he was a researcher in Tokyo Institute of Technology. From 2016 to 2018, he was with Tokyo University of Science as an assistant professor. From 2018 to 2022, he was with The University of Tokyo as an assistant professor/research-intensive lecturer. Since 2022, he has been with IMEC Netherlands as a researcher. His research interests include data converters, PLLs, oscillators, and their design automation. Dr. Xu is a member of the IEEE. He is serving as a technical program committee member of IEEE A-SSCC. From 2017 to 2022, he was an associate editor of IEICE transactions. Dr. Xu is the recipient of NEWCAS best student paper award in 2013, CICC student scholarship award in 2013, and Yasujiro Niwa Outstanding paper award in 2017.

Takehito Ishii received B.E. degree in Electronics Engineering from Tokyo University of Science, Tokyo, Japan, in 1996. He was engaged in the design of VCOs and RF modules of UHF band at Murata Manufacturing, Shiga, Japan, from 1996 to 2003, and at Nihon Dempa Kogyo, Saitama, Japan, from 2003 to 2020. Since 2020, he has been a Principal Engineer at Piezo Studio, Saitama, Japan. His research interests include the design of low power oscillation circuits with piezoelectric devices and wireless telecommunication equipment using the above oscillators. He is the 1st-Class Technical Radio Operator for On-The-Ground Services, Japan.

Noritoshi Kimura graduated from Akita National College of Technology, Akita, Japan, in 1987. He received B.E. and M.E. degree in Electronics Engineering from Akita University, Akita, Japan, in 1990 and 1992 respectively, and Ph.D. degree in Electrical and Communication Engineering, Tohoku University, Sendai, Japan, in 1999. After working at TDK, Chiba, Japan and Samsung Electro-Mechanics, Suwon, Korea, he joined Nihon Dempa Kogyo, Saitama, Japan, in 2003, and was an Executive Officer, in 2014. In 2018, he joined Piezo Studio, Sendai, Japan, as a Director, and has been CEO since 2019. His research interests are SAW devices and Quartz timing devices using MEMS technology. He is a Senior Member of IEICE and a Member of IEEE.