Evaluation of a True Random Number Generator Utilizing Timing Jitters in RSFQ Logic Circuits

Kenta SATO††, Naonori SEGA†, Student Members, Yuta SOMEI†, Hiroshi SHIMADA†, Nonmembers, Takeshi ONOMI††, and Yoshinao MIZUGAKI(b), Members

SUMMARY We experimentally evaluated random number sequences generated by a superconducting hardware random number generator composed of a Josephson-junction oscillator, a rapid-single-flux-quantum (RSFQ) toggle flip-flop (TFF), and an RSFQ AND gate. Test circuits were fabricated using a 10 kA/cm² Nb/AIOₓ/Nb integration process. Measurements were conducted in a liquid helium bath. The random numbers were generated for a trigger frequency of 500 kHz under the oscillating Josephson-junction at 29 GHz. 26 random number sequences of 20 kb length were evaluated for bias voltages between 2.0 and 2.7 mV. The NIST FIPS PUBS 140-2 tests were used for the evaluation. 100% pass rates were confirmed at the bias voltages of 2.5 and 2.6 mV. We found that the Monobit test limited the pass rates. As numerical simulations suggested, a detailed evaluation for the probability of obtaining “1” demonstrated the monotonical dependence on the bias voltage.

key words: Single-flux-quantum logic circuit, Hardware random number generator, Nb integration

1. Introduction

Single-flux-quantum (SFQ) digital circuitry is a superconductive technology [1]–[4] realizing high-speed operation (i.e., up to subterahertz for Nb/AIₓ/Nb integrated circuits) with low power consumption (i.e., four orders of magnitude less than that of CMOS circuits) [5], [6]. A number of journal papers/technical reports on SFQ-based digital circuits demonstrating these features, such as [7]–[9], have been published.

In addition to digital computing elements, random number generators are another application of SFQ circuits [10], [11]. Random number sequences are used in various fields such as statistical analysis, simulations of natural phenomena, wireless communication, and cryptographic communication. There are two ways to generate random numbers: utilizing a mathematical algorithm and a random physical phenomenon. Random numbers generated by a mathematical algorithm are pseudo random. Although they are periodical and thus predictable, they are widely used for long periods to ensure practical unpredictability. A lot of SFQ-based pseudo-random number generators have been proposed and operated [10], [12]–[15]. On the other hand, random numbers that a physical phenomenon (i.e., thermal noise, atom collapse, and chaotic dynamics) generates is truly random, resulting in ideal nonperiodicity and unpredictability. Due to their generation methods, true random numbers are generated only by hardware random number generators (HRNGs). HRNGs composed of SFQ-based circuits were demonstrated in which thermal noises were utilized [11], [16].

We recently proposed an oscillation-based HRNG in which timing jitters in SFQ digital circuits were employed [17]. The oscillation-based HRNG was composed of a few logic gates and the Josephson oscillator using the Josephson relationship between the voltage and oscillation frequency. Due to its simple configuration, the oscillation-based HRNG was realized in SFQ circuitry with low hardware costs and technical difficulty. We designed and fabricated test circuits using the digital cell library (referred to as “CONNECT” [18]) and the 2.5 kA/cm² Nb/AIOₓ/Nb integration process (STP2) [19] of the National Institute of Advanced Industrial Science and Technology (AIST), and confirmed that random numbers generated by a test circuit satisfied all criteria of the NIST FIPS PUBS 140-2 (hereafter, referred to as FIPS 140-2) tests [20]. However, our test at that time was conducted only for one biasing condition.

In this paper, we refer to our oscillation-based HRNG as an “SFQ oscillation-based HRNG,” of which the abbreviation is “SO-HRNG.” We transfer the design of the original SO-HRNG from STP2 to the 10 kA/cm² Nb/AIOₓ/Nb integration process (HSTP) of AIST [21]. Higher random number generation rates are expected using SFQ circuitry with larger critical current densities even though we do not attempt high-speed random number generation in this paper. Test circuits fabricated using the HSTP are evaluated through the FIPS 140-2 tests with various biasing conditions. The dependence of the random number quality on the biasing conditions is discussed.

2. Configuration of the SO-HRNG

Figure 1 shows a simplified configuration of the SO-HRNG [17]. The circuit consists of an over-biased Josephson junction, a toggle flip-flop (TFF), and an AND gate. The over-biased Josephson junction, which is in the voltage state by injecting DC current larger than the junction critical current, works as an oscillator generating SFQ pulses with the repetition-frequency \( f = \frac{V}{\Phi_0} \), where \( V \) and \( \Phi_0 \) are the DC voltage across the junction and the quantity of an SFQ [22]. The high repetition-frequency SFQ pulses are trans-
Fig. 1  Simplified block diagram of the SFQ oscillation-based HRNG (SO-HRNG)

ferred from the over-biased Josephson junction to the input
terminal of the TFF and the clock terminal of the AND gate.
Moreover, the TFF provides one SFQ pulse to a signal input
terminal of the AND gate for every two input SFQ pulses.
Then, the internal state of the AND gate switches between
“0” and “1” at the oscillation frequency of the over-biased
Josephson junction. Meanwhile, trigger SFQ pulses of low
repetition-frequency are fed to another input terminal of the
AND gate. If the internal state of the AND gate is “0” (or “1”)
at the timing of the trigger SFQ arrival, the output becomes
“0” (or “1”) for the subsequent clock signal. If there were no
noise effects in the circuits, there should be synchronous op-
eration of the high repetition-frequency SFQ pulses from the
over-biased Josephson junction and the low-frequency SFQ
pulses from the trigger terminal. However, thermal noise
currents at finite temperatures must induce timing jitters in
the trigger signal line, leading to a true random number out-
put.

It should be noted that, the timing jitters should
be larger than the oscillation period of the over-biased Joseph-
son junction to generate true random numbers. Numerical
simulation using “jsim_n”[23] for the SO-HRNG at 4.2 K
with the parameters of the HSTP suggested that the trigger
frequency reached no less than 400 MHz under the over-
biased Josephson junction oscillating at 150 GHz.

3. Experiments

The SO-HRNG was designed using a digital cell library,
the modified “CONNECT” library for the AIST HSTP. A
DC-to-SFQ converter and an SFQ-to-DC converter were im-
plemented for the SO-HRNG in addition to the over-biased
Josephson junction, TFF, and AND gate shown in Fig. 1.

Test chips were fabricated using the AIST HSTP. Figure
2 shows a photomicrograph of a fabricated SO-HRNG.

In measurements, a test chip was cooled in a liquid
helium bath. The trigger input was a sine wave fed from
a function generator to a DC-to-SFQ converter via a 50 Ω
resistor on the chip. The DC voltage across the over-biased
Josephson junction was set to 60 µV, of which the corre-
sponding oscillation frequency was 29 GHz. The output
signal from the SFQ-to-DC converter was monitored and
observed with a digital oscilloscope via a 40-dB
preamplifier. We chose the trigger frequency as 500 kHz
since the cut-off frequency of the preamplifier was 1 MHz.

Test sets defined in the FIPS 140-2 tests (Monobit,
Poker, Runs 1–Runs 6+, and Long Runs) [20] were again
used to evaluate the quality of random numbers generated by
the SO-HRNG. Notably, the FIPS 140-2 testing has ended,
and other improved tests such as NIST SP800-22[24] and
TestU01[25] are now available. However, the other modern
tests require 10–1000 Mb random numbers, which were be-
Yond the capacity of the storage in the digital oscilloscope.
The trigger frequency of 500 kHz was not high enough, ei-
ther. Due to these limitations in our experimental setup, we
chose the FIPS 140-2 tests for evaluation.

26 random number sequences of 20 kb length were
acquired and evaluated for each biasing condition.

4. Results and Discussion

Figure 3 presents an example of the SO-HRNG operation. It
should be noted that each high/low transition of the SFQ-to-
Bias converter represents an output of “1,” while no transition at a rising edge of the trigger signal means “0”. Therefore, Fig. 3 exhibits a bit sequence of “011010100100101011100,” demonstrating a typical random number sequence.

Figure 4 displays the bias voltage dependence of the pass rate for the FIPS 140-2 tests. As a result, the pass rate became 100% at 2.5 and 2.6 mV, and the nominal bias voltage of the cell library was 2.5 mV. That is, 26 random number sequences of 20 kb length generated by the SO-HRNG at the biasing conditions of 2.5 and 2.6 mV satisfied all criteria of the FIPS 140-2 tests. As the biasing condition moves far from the nominal value, the pass rates gradually deteriorate below 2.5 and above 2.6 mV.

Furthermore, the pass rate for each test at each biasing condition is presented in Fig. 5. The pass rates for nine tests are plotted as functions of the bias voltage.

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Furthermore, the pass rate for each test at each biasing condition is presented in Fig. 5. The pass rates for the Runs 1–Runs 6+ and Long Runs tests are 100% for the biasing conditions between 2.0 and 2.7 mV, whereas those for the Poker test reach 100% between 2.2 and 2.7 mV. Conversely, the Monobit test was 100% satisfied for the limited conditions of 2.5 and 2.6 mV. Additionally, the Monobit test checks if the number “1” in a 20 kb sequence falls into the range between 9,725 and 10.275. From Fig. 5, it is determined that the Monobit test is the most challenging test for the SO-HRNG.

Further evaluation for the Monobit test is shown in Fig. 6. Consequently, the probability of getting “1” was increased monotonically with increasing the bias voltage. Such bias dependence was in agreement with our numerically results [26], as discussed below. For the bias voltages of 2.5 and 2.6 mV, the “1” probabilities of all 26 random number sequences of 20 kb length satisfied the criteria (between 48.725 and 51.275%). For other biasing conditions, some random number sequences did not satisfy the Monobit requirements in the FIPS 140-2.

Numerical simulation in our previous work [26] figured out that the AND gate had different switching areas for the outputs of “0” and “1” and that they depended on the bias voltage. In the SO-HRNG shown in Fig. 1, the time duration ratio for the AND gate generating “1” and “0” should ideally be 50%:50% for two clock periods. However, the time duration ratio for the AND gate in the “CONNECT” library changes from 49.88%:50.12% to 50.05%:49.95% as the bias voltage increases from 2.2 to 2.7 mV. More specifically, numerical results signified that the ratio for the output of “1” increased as the bias voltage increased, consistent with the experimental results shown in Fig. 6. In order to improve the bias margin of the SO-HRNG in the future, the bias dependence of the AND gate should be addressed.

5. Conclusion

We experimentally evaluated random number sequences generated by the SO-HRNG. Test circuits were fabricated using the AIST HSTP (10 kA/cm²). Measurements were conducted in a liquid helium bath. 26 random number sequences of 20 kb length were evaluated for bias voltages between 2.0 and 2.7 mV. The FIPS 140-2 tests were used for evaluation, where 100% pass rates were confirmed at bias voltages of 2.5 and 2.6 mV. We determined that the Monobit test limited the pass rates. Detailed evaluation for the probabilities of getting “1” showed the monotonical dependence on the bias voltage as numerical simulation had suggested. The bias voltage dependence was likely to be attributed to the characteristics of the AND gate.
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