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SUMMARY This paper proposes a topology of high power, MHz-frequency, half-bridge resonant inverter ideal for low-loss Gallium Nitride high electron mobility transistor (GaN-HEMT). General GaN-HEMTs have drawback of low drain-source breakdown voltage. This property has prevented conventional high-frequency series resonant inverters from delivering high power to high resistance loads such as 50Ω, which is typically used in radio frequency (RF) systems. High resistance load causes hard-switching also and reduction of power efficiency. The proposed topology overcomes these difficulties by utilizing a proposed ‘L-S network’. This network is effective combination of a simple impedance converter and a series resonator. The proposed topology provides not only high power for high resistance load but also arbitrary design of output wattage depending on impedance conversion design. In addition, the current through the series resonator is low in the L-S network. Hence, this series resonator can be designed specifically for harmonic suppression with relatively high quality-factor and zero reactance. Low-distortion sinusoidal 3kW output is verified in the proposed inverter at 13.56MHz by computer simulations. Further, 99.4% high efficiency is achieved in the power circuit in 471W experimental prototype.

key words: resonant inverter, GaN-HEMT, ISM bands, impedance conversion, harmonics suppression.

1. Introduction

This study aims for generating a high frequency, high power, low distortion sinusoidal wave with low power loss. High frequency inverters are necessary for MHz-frequency applications such as plasma processing systems and wireless power transfer (WPT) operated in the industrial, scientific, and medical (ISM) frequency bands. Gallium Nitride high electron mobility transistor (GaN-HEMT) should be suitable for such inverters due to its low loss and high-speed switching ability [1]–[5]. However, the use of silicon transistors is the mainstream, and GaN-HEMTs have not yet been fully put into practical use in high-frequency systems. One of the reasons is because the drain-source breakdown voltage of commercially available GaN-HEMTs is as low as 650V at maximum.

Class-E topology has been attracting great deal of attentions in recent years as high-frequency inverter [4]–[8]. Nonetheless, class-E topology has a problem of high drain-source voltage, which becomes an obstacle to high output power using GaN-HEMTs. In addition, a DC input inductor required as a current source in class-E topology tends to have high power loss. Then, the authors focus on half-bridge topology having drain-source voltage stability due to its voltage-source characteristic. In an ideal half-bridge with no parasitic parameters, the drain-source voltage never exceeds the input DC voltage.

Half-bridge and full-bridge series resonant inverters [9] have been prominent solutions for generating various ranges of power with relatively low frequency [10]–[19]. These inverters have the advantages of low loss zero voltage switching (ZVS) and drain-source voltage stability against load fluctuations [20]. However, the load voltage amplitude by the conventional half-bridge topology is only half of the drain-source voltage. In order to obtain high output power with low voltage GaN-HEMT, the load current must be large. Actually, large current cannot be achieved since load resistance used in high-frequency applications is large such as 50Ω generally. Hard-switching is also a problem caused by small current. Whereas, if a low resistance load is used, large current flows through the series resonator, and remarkable high loss is caused in the series resonator. The design to meet the requirements of ZVS and harmonic suppression becomes difficult.

This paper overcomes these difficulties by using the proposed passive ‘L-S network’. This network meets the design requirements of ZVS, low output harmonics, and high power with low loss without raising drain-source voltage. The L-S network consists of an impedance converter ‘L-network’ as the front stage and a series resonator as the rear stage. The half-bridge ensures the stability of the drain-source voltage, the impedance converter achieves high output power and ZVS operation simultaneously, and the series resonator suppresses harmonics. Each function is established under a specialized independent design of each component.

By utilizing the impedance conversion, the output power wattage can be designed in a wide range. Theoretically, kW-power is possible without limited from drain-source voltage, input DC voltage, and load resistance. In addition, the current flowing in the series resonator is reduced by the impedance converter. This is because in the impedance converter is located in the front stage of the series
As mentioned above, clear division and specialization of each function bring high degree of freedom in design and the resulting improvement in the performance of the entire inverter circuit, and the requirements are met. This is the important point the authors would like to emphasize most about the proposed topology. This paper also reports on experimental prototype design details, including ideas for bypass capacitors to avoid ringing. Table 1 shows the achievements of this study.

**Table 1 Achievements of this study.**

| Enhanced flexibility of output wattage design. |
| Enhanced flexibility in design of quality-factor for harmonics suppressions. |
| High output power with low drain-source voltage of GaN-HEMTs. |
| High output power with low input DC voltage. |
| High output power for high resistance load 50Ω fixed in standard RF systems. |
| High efficiency over 99% at 13.56MHz. |
| Sinusoidal output wave with low distortions. |

This paper is divided into seven sections: Section 2 discusses about the problems of the conventional series resonant inverter. In section 3, the advantages, operation principles, and design of the proposed inverter are explained. Section 4 reports the simulation results. Section 5 describes about the experimental prototype. Section 6 shows the experimental results. Section 7 is the conclusion.

## 2. Conventional Half-Bridge Series Resonant Inverter

The circuit diagram of the conventional high-frequency half-bridge resonant inverter is shown in Fig. 1. The symbols S1 and S2 mean GaN-HEMT power switches, and D1 and D2 mean additional Silicon Carbide Schottky-barrier diodes (SiC-SBD) connected to S1 and S2 in reverse-parallel. D1 and D2 are not essential because GaN-HEMT is capable of reverse conduction. However, the reverse voltage drop of GaN-HEMT could reach several volts, causing waveform distortions and power loss in S1 and S2. These problems can be mitigated by implementing D1 and D2 having lower forward voltage drops. SiC-SBD is suitable for D1 and D2 because it has not only low voltage drop but also small parasitic capacitance and fast response. The series capacitor \( C_S \) and the inductor \( L_S \) make a series resonator which has a combined reactance \( X_S \). \( X_S \) must be designed as a positive value; inductive reactance to achieve ZVS operations in S1 and S2. Phase-angle \( \theta \) binds \( X_S \) and \( R_{\text{load}} \) as (4).

\[
X_S = R_{\text{load}} \tan \theta \tag{4}
\]

The output power of this inverter is expressed as (5) using \( \theta \)

\[
P_{\text{out}} = \frac{\left( \frac{4}{\pi} \times \frac{V_{\text{DC}}}{2} \right)^2}{2R_{\text{load}}(1 + \tan^2 \theta)} \tag{5}
\]

where \( V_{\text{DC}} \) and \( R_{\text{load}} \) are the DC power supply voltage and load resistance. \( V_{\text{DC}} \) value is equal to drain-source voltage of off-period. In practical applications, voltage surges can occur during hard-switching due to load fluctuations. Therefore, it is desirable to keep \( V_{\text{DC}} \) to less than half of the GaN-HEMT drain-source breakdown voltage.

![Fig. 1 Circuit diagram of the conventional half-bridge resonant inverter.](image)

Hence, \( P_{\text{out}} \) is necessarily limited by \( R_{\text{load}} \) and \( V_{\text{DC}} \). For example, when the parameters are \( R_{\text{load}}=50\Omega \), \( V_{\text{DC}}=280V \), and \( \theta=\pi/5\text{rad} \), \( P_{\text{out}} \) is derived as 208.0W, and it cannot reach to higher such as kW-power.

In addition, low current due to high resistance \( R_{\text{load}} \) causes hard-switching in GaN-HEMTs, which reduces power efficiency and increases heat generation. This is also one of the causes of the difficulty of high output power. In order to avoid or reduce hard-switching, high inductive reactance is necessary on the series resonator. However, this method causes a large voltage drop in the series resonator because its resonance frequency deviates significantly from the switching frequency.

As a method of high output power to a high resistance load with a low drain-source voltage in the kHz-frequency applications, inserting a step-up transformer between the series resonator and the load has been studied [14]–[19]. Nonetheless, in the MHz-frequency application, power-loss due to high-frequency large excitation current in the transformer [21] and high-frequency large current in the series resonator increase. This problem makes it difficult to design passive components and achieve high efficiency.

Fig. 2 illustrates the operating waveforms of this inverter. Note that, drain currents \( i_{\text{SBD}\text{-high side}} \) and \( i_{\text{SBD}\text{-low side}} \) include currents flowing through parasitic capacitances of S1 and S2. The gate signals \( v_{gs\text{-high side}} \) and \( v_{gs\text{-low side}} \) have the same duty-cycles and dead-times, and drive S1 and S2 alternately. Positive \( X_S \) causes the phase lagging of \( i_{\text{SBD}\text{-high side}} \) and \( i_{\text{SBD}\text{-low side}} \) to drain-source voltages \( V_{ds\text{-high side}} \) and \( V_{ds\text{-low side}} \). \( i_{\text{SBD}\text{-high side}} \) and \( i_{\text{SBD}\text{-low side}} \) are currents across reverse-parallel diodes. ZVS turn-on is achieved when S1 or S2 is turned on at current \( i_{\text{SBD}\text{-high side}} \) or \( i_{\text{SBD}\text{-low side}} \) is flowing through D1 or D2. The output current \( i_{\text{out}} \) is not pure sine wave and has distortions caused by turn-off operations.

![Fig. 2 Waveforms in the conventional half-bridge resonant inverter.](image)
3. Proposed Inverter

3.1 Significance of the Proposed Topology

The proposed inverter has an ability of output high power without being restricted from drain-source voltage and load. In the proposed topology, an impedance converter called L-network is inserted between half-bridge switch and output series resonator as shown in Fig. 3. The authors named this passive network as ‘L-S network’. The proposed L-S network enables separating the circuit design for noise suppression from those for impedance conversion and high output power. This flexibility on circuit design enables high output power of high-frequency sinusoidal waves. The output power wattage is determined by the impedance conversion design of the L-network. It can deliver high output power to high resistance loads, expanding the range of applications compared to conventional converters.

![Fig. 3 Circuit diagram of the proposed L-S inverter.](image)

Further, the L-network is also utilized as inductive reactance for achieving ZVS operation of GaN-HEMT switches S1 and S2. The L-network and series resonator can be designed independently in the proposed topology. ZVS is easily achieved because half-bridge current is large, and electric charges of output capacitance of the switch S1 or S2 are strongly withdrawn in turn-on periods. Although large drain currents flow in S1 and S2, this is not a problem because it is assumed that GaN-HEMTs having allowable current of tens of amperes are used.

Unlike in the conventional half-bridge series resonant topology, the inductive reactance for ZVS operation is provided by the L-network not by the series resonator, in the proposed L-S network. The series resonator is not involved in ZVS operations in the proposed inverter topology. Therefore, the reactance $X_S$ of the series resonator can be designed as zero at the switching frequency. $X_S=0$ enables the switching frequency to be matched to the maximum power transfer point of the series resonator to the load. Narrowing the resonator bandwidth does not reduce the transmission rate due to reactance. In addition, large current does not flow in the series resonator because this resonator is located after the impedance converter. For these reasons, high quality-factor is applicable to the series resonator without severe restrictions. The proposed topology is advantageous especially in ISM bands applications over the conventional topology because it can provide higher transmission ability and output power even in very narrow bandwidth.

The proposed L-S network has the same appearance as the existing ‘LCCL compensation architecture’ that is becoming popular in the study of low-frequency WPT such as 85kHz [22]–[24]. However, the proposed L-S network is not conceived or derived from the LCCL compensation and has different purposes. The proposed L-S topology is devised for the purpose of preventing overvoltage of GaN-HEMT and avoiding hard-switching, and aims to maximize the ability of GaN-HEMT in power. Various implementations for MHz-frequency power transfer with compensation methods continue to be proposed [25]–[29], and consensus for design is insufficient. Moreover, if the LCCL compensation architecture is used in the MHz-frequency high power WPT system, the concept and design method of the proposed topology can be applied directly, and can contribute to the stable use of GaN-HEMT in such WPT system.

Fig. 4 illustrates the operating waveforms of the proposed inverter. The operations for the transistors are the same as the conventional inverter. However, the drain currents $i_{d_{\text{high-side}}}$ and $i_{d_{\text{low-side}}}$ are larger than those of conventional circuit. $i_{\text{hsb}}, i_{\text{L}-\text{nets}}$ and $i_{\text{out}}$ are the currents from half-bridge configuration, capacitor $C$ in the L-network, and inverter output to the load resistor, respectively. Unlike in the conventional topology having only the series resonator, $i_{\text{out}}$ distortion is very small in the proposed topology because harmonics is suppressed in both the L-network and the series resonator, and the series resonator has higher quality factor.

![Fig. 4 Waveforms in the proposed L-S inverter.](image)

3.2 Design for High Power and ZVS

The impedance converter L-network can be designed to provide high performance because it should meet only the requirements of high output power and ZVS. Appropriate design of the L-network enables to withdraw high power from a DC supply through the half-bridge switch. The important parameters to determine the withdrawn power are the input resistance $r_i$ and reactance $X_M$ of the L-network. It is not necessary to give a high inductance and high quality-
factor to the L-network because noise suppression requirement can be met exclusively by the series resonator. It is generally known that the power loss can be made much smaller than the input or output power of the circuit by using low-loss components such as GaN-HEMTs and high-purity thick copper wire inductors. Since the main purpose of this section is to design high output power, small power losses are omitted to simplify the discussion. In this case, the output RF power $P_{out}$ is determined as (6) because $P_{out}$ is equal to the input power drawn from the DC power supply.

\[
P_{out} = \left( \frac{4}{\pi} \times \frac{V_{DC}}{2} \right)^2 \frac{r_{in}}{2(r_{in}^2 + x_{in}^2)}
\]  

(6)

$P_{out}$ wattage can be designed widely depending on the design parameters of the L-network. $x_{in}$ is determined as (7) by $r_{in}$ and the positive phase-angle $\theta$ for achieving ZVS operation.

\[
x_{in} = r_{in} \tan \theta
\]  

(7)

Though the impedance conversion theory is effective in sinusoidal wave circuits, the inverter uses rectangular waves in drain-source voltages. Then, the coefficient $r_{in}$ can be derived from the target value of $P_{out}$. $r_{in}$ and $x_{in}$ are designed as low enough to draw a large current.

Next, the required values of $r_{in}$ and $x_{in}$ are realized by designing the inductance L and capacitance C of the L-network. When $X_S$ is designed as zero, the input impedance $z_{in}$ of the L-network is expressed as (10) by using $L$, $C$, and the load resistance $R_{load}$.

\[
z_{in} = j\omega_0 L + \frac{R_{load}}{\frac{1}{\omega_0 C} + R_{load}}
\]  

(10)

where $\omega_0$ is the switching angular frequency. By rearranging (10), $C$ and $L$ are derived as (11) and (12) from $r_{in}$ and $x_{in}$.

\[
C = \frac{1}{\omega_0^2} \left( \frac{1}{r_{in}R_{load}} - \frac{1}{R_{load}^2} \right)
\]  

(11)

\[
L = \frac{x_{in}}{\omega_0^2} + \frac{C R_{load}^2}{1 + \omega_0^2 C^2 R_{load}^2}
\]  

(12)

All parameters to output $P_{out}$ are determined by (7)–(12). For example, when the required values are $P_{out}=3$ kW, $R_{load}=50\Omega$, $\omega_0=2\pi \times 13.56$ MHz, and $\theta=\pi/5$ rad, the parameters are determined as $r_{in}=3.466\Omega$, $x_{in}=2.518\Omega$, $L=0.179\mu\text{H}$, and $C=860.1\text{pF}$. $L$ and $C$ can be also determined by using a Smith chart as shown in Fig. 5.

In the actual circuit construction on a printed circuit board (PCB), $C$ should include the stray capacitance of PCB, $L$ should include the parasitic inductance of pathways on the PCB such as return-path on a ground plane.

![Fig. 5 Impedance conversion design of the L-network by Smith chart.](image)

3.3 Design for Harmonics Suppression

Since operating frequencies of the high-power MHz-frequency applications are generally limited within the ISM bands, harmonics suppression is necessary. In the proposed topology, the series resonator can be designed to be specialized only for suppressing noises other than the switching frequency wave. This series resonator is utilized as bandpass filter to output sinusoidal wave. Its design and structure are very simple compared to implementing a filter network such as a Chebyshev filter as [13], [14].

As highlighted in the section 3.0, the series resonator in the proposed topology can be designed independently of the impedance transducer. $X_S$ needs not to be inductive in the proposed topology because ZVS operation is achieved by the inductive L-network. Therefore, $X_S$ can be designed as zero by $\omega_0 L_S=1/\omega_0 C_S$, and voltage drop on the resonator is minimized at the switching frequency.

In the proposed topology, smaller current flows in the series resonator, unlike in the L-network. Therefore, it is possible to use a resonant inductor having a large number of turns and a magnetic core. The inductor power-loss is low, and a high quality-factor are given due to its high inductance $L_S$. The loaded quality-factor $Q_S$ of the series resonator with the load $R_{load}$ affects the amplitudes of harmonics. Unlike in the conventional half-bridge series resonant topology, $Q_S$ is independent from requirements of ZVS operation. $Q_S$ is expressed as (13) or (14) at the switching frequency $f_0$.

\[
Q_S = \frac{1}{R_{load}} \left( \frac{L_S}{C_S} \right)
\]  

(13)

\[
Q_S = \frac{2\pi f_0 C_S R_{load}}{1}
\]  

(14)

$Q_S$ influences on the AC voltage amplitude $V_{CS}$ applied to the resonant capacitor $C_S$. $V_{CS}$ is an important parameter in considering the breakdown voltage of the capacitor $C_S$. $V_{CS}$ is expressed as (15) by using (14).

\[
V_{CS} = \frac{f_{out}}{2\pi f_0 C_S} = Q_S R_{load} f_{out}
\]  

(15)
where $I_{out}$ is resonance current amplitude in the series resonator. The influences of harmonic currents on $V_{CS}$ are negligible. $V_{CS}$ and $Q_S$ were simulated using the computer simulation described later. $L_S$ and $C_S$ can be determined based on (13), (14), and (15).

4. Computer Simulation

4.1 Output Power and Circuit Operations

The proposed inverter was simulated to verify the theoretically designed high output power and ZVS operation. Computer simulations of the proposed circuit were implemented using the PLECS software. The simulated circuit parameters designed for 3kW output are listed in Table 2. $V_{DC}=280\text{V}$ results in the drain-source voltage amplitude of 280V due to the voltage-source half-bridge topology. The detailed parameters such as on-resistance $R_{on,FET}$, drain-source output capacitance $C_{OSS}$ of the switches S1 and S2, and the parasitic capacitance $C_{SBD}$ of the SBD are based on the datasheets [30], [31] of the GS66516B GaN-HEMT and the C3D03065E SBD. The circuits were compared with and without $C_{OSS}$ and $C_{SBD}$. This is because these capacitances were likely to incur significant switching loss.

The simulation results show that, the average output power $P_{out}$ is 2.950kW, and the high output power of the proposed inverter is confirmed. As shown in Table 2, the power efficiency $\eta$ including $C_{OSS}$ and $C_{SBD}$ is 99.12%, and it is revealed that $C_{OSS}$ and $C_{SBD}$ cause only a slight drop of $P_{out}$ compared to the case with no parasitic capacitances. The powers and efficiency listed in Table 2 are the average of one cycle in the steady state.

Table 2 Designed and resulted parameters of the simulation.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input DC voltage (V)</td>
<td>$V_{DC}$</td>
<td>280</td>
</tr>
<tr>
<td>Drain-source voltage amplitude (V)</td>
<td>$V_o$</td>
<td>280</td>
</tr>
<tr>
<td>Load resistance (Ω)</td>
<td>$R_{load}$</td>
<td>50</td>
</tr>
<tr>
<td>Switching frequency (MHz)</td>
<td>$f_{sw}$</td>
<td>13.56</td>
</tr>
<tr>
<td>Duty cycles including dead times</td>
<td>$D$</td>
<td>0.43</td>
</tr>
<tr>
<td>Dead time of each gating signal (ns)</td>
<td>$t_d$</td>
<td>5.0</td>
</tr>
<tr>
<td>ON-resistance of transistor (mΩ)</td>
<td>$R_{on,FET}$</td>
<td>25</td>
</tr>
<tr>
<td>ON-resistance of SBD (mΩ)</td>
<td>$R_{on,SBD}$</td>
<td>200</td>
</tr>
<tr>
<td>Forward voltage of SBD (V)</td>
<td>$V_{ds}$</td>
<td>1.8</td>
</tr>
<tr>
<td>Output capacitance of transistor (pF)</td>
<td>$C_{OSS}$</td>
<td>150</td>
</tr>
<tr>
<td>Parasitic capacitance of SBD (pF)</td>
<td>$C_{SBD}$</td>
<td>11</td>
</tr>
<tr>
<td>Inductance in the L-network (µH)</td>
<td>$L$</td>
<td>0.179</td>
</tr>
<tr>
<td>Capacitance in the L-network (pF)</td>
<td>$C_L$</td>
<td>860.1</td>
</tr>
<tr>
<td>Capacitance in the series resonator (pF)</td>
<td>$C_S$</td>
<td>137.8</td>
</tr>
<tr>
<td>Inductance in the series resonator (µH)</td>
<td>$L_S$</td>
<td>1.0</td>
</tr>
<tr>
<td>Output power (theoretical) (kW)</td>
<td>$P_{out}$</td>
<td>3.0</td>
</tr>
</tbody>
</table>

Fig. 6 shows the simulated waveforms; ‘L current $i_L$’ and ‘C current $i_C$’ are currents in the inductor and capacitor of the L-network, ‘Output power $P_{out}$’ is power fed to the 50Ω load, ‘D1 current $i_{SBD1}$’ and ‘D2 current $i_{SBD2}$’ are currents across the reverse-parallel SBDs of high-side and low-side switches, and ‘$C_{OSS1}$ current’ and ‘$C_{OSS2}$ current’ are the current across the parallel capacitances composed of $C_{OSS}$ and $C_{SBD}$.

In each turn-off operation of the switch S1 and S2, current in $C_{OSS}$ does not consume energy but only charges $C_{OSS}$. In the turn-on operation, the drain-source voltage ‘$V_{ds1}$’ or ‘$V_{ds2}$’ falls to zero before the drain channel current ‘$i_{ds1}$’ or ‘$i_{ds2}$’ starts to flow. In other words, $C_{OSS}$ and $C_{SBD}$ are discharged before current flows to the drain channel, and ZVS operation is achieved obviously. The spikes seen on ‘$C_{OSS1}$ current’ and ‘$C_{OSS2}$ current’ are caused by slight reverse voltage of $C_{OSS}$ and $C_{SBD}$ charged by forward voltage drop in the reverse-parallel diode D1, D2.

In the simulation, the simulation models of the power switches S1 and S2 are ideal switches which have 25mΩ on-resistance but no turn-off and turn-on delays in the drain-source channel. In the real power switch, the channel resistance will increase during the turn-on and turn-off periods, and it will cause switching loss. However, this loss generation effect is little in GaN-HEMT because the turn-on and turn-off speeds are very fast. Hence, almost all amounts of current will not flow across the channel but across $C_{OSS}$ or $C_{SBD}$ during a dead-time.

4.2 Output Harmonics

The relation between $Q_S$ and harmonics was also investigated in the simulation to evaluate the harmonics suppression ability and the resonant voltage of the L-S network. $L_S$ and $C_S$ are changed in this simulation, but other parameters are same with the values in Table 2. The fundamental frequency is 13.56MHz.

Simulation results are shown in Table 3 and Fig. 7. Depending on $Q_S$ value, the voltage of fundamental 13.56MHz wave are almost constant, but the relatively
remarkable 3rd and 5th harmonics voltages decrease and \( V_{CS} \) increases as listed in Table 3. Fig. 7 illustrates the relation between \( Q_s \), 2nd to 11th harmonics voltages, and \( V_{CS} \). Dotted curves of 3rd, 5th, and 7th harmonics in Fig. 7 are the approximation curves estimated from the plotted data. The harmonics voltages other than the 3rd, 5th, and 7th harmonics are quite low as 18mV or less, which is almost zero in the graph. According to the results, higher \( Q_s \) causes lower harmonic voltages but higher \( V_{CS} \); \( V_{CS} \) is proportional to \( Q_s \) as shown in Fig. 7. When \( Q_s \) is 4.0, \( V_{CS} \) exceeds 2kV, and RF capacitors with high breakdown voltage are necessary; such capacitors tend to be very expensive. Thus, the series resonator should be designed with considering the trade-off relation in harmonics and \( V_{CS} \).

### Table 3  Simulation results of harmonics and capacitor voltages.

<table>
<thead>
<tr>
<th>( Q_s )</th>
<th>( L_s (\mu H) )</th>
<th>( C_s (pF) )</th>
<th>13.56 MHz</th>
<th>3rd harmonic</th>
<th>5th harmonic</th>
<th>( V_{CS} (V) )</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.0</td>
<td>0.587</td>
<td>234.7</td>
<td>541.0</td>
<td>2.322</td>
<td>0.256</td>
<td>6813</td>
</tr>
<tr>
<td>1.5</td>
<td>0.800</td>
<td>156.5</td>
<td>541.0</td>
<td>1.591</td>
<td>0.175</td>
<td>9550</td>
</tr>
<tr>
<td>2.0</td>
<td>1.174</td>
<td>117.3</td>
<td>540.9</td>
<td>2.025</td>
<td>0.135</td>
<td>1223</td>
</tr>
<tr>
<td>3.0</td>
<td>1.761</td>
<td>78.23</td>
<td>541.0</td>
<td>0.807</td>
<td>0.091</td>
<td>1764</td>
</tr>
<tr>
<td>4.0</td>
<td>2.347</td>
<td>58.70</td>
<td>541.0</td>
<td>0.609</td>
<td>0.069</td>
<td>2304</td>
</tr>
</tbody>
</table>

![Fig. 7] Simulation results of capacitor voltage and 2nd to 11th harmonics.

### 5. Experimental Prototype

#### 5.1 Overview of the Prototype

Fig. 8 shows the prototype of the proposed inverter. Fig. 9 shows the circuit diagram of the power circuit of the prototype. The devices and passive components implemented in the prototype are listed in Table 4. The operating frequency is 13.56MHz. The power switches consisting in the half-bridge are GS66516B GaN-HEMTs, and the external reverse-parallel SBDs are C3D03065E. The load used in this experiment is a RF 50Ω oil-cooled load whose resistance was measured as 50.37Ω at 13.56MHz by using an IM7581 impedance analyzer. This value includes the parasitic resistance of the coaxial cable that connects inverter and load resistor.

The inputted power \( P_{in} \) in this experiment was about 470W because the prototype has not enough ability in heat dissipation for the high-side switch S1. The output voltage \( V_{out} \) of the inverter was measured by at the same point which the load resistance \( R_{load} \) is measured. The output power \( P_{out} \) was acquired by \( P_{out} = \frac{V_{out, RMS}^2}{R_{load}} \) where \( V_{out, RMS} \) is effective output voltage. The parameters of the components of the prototype are listed in Table 5.

![Fig. 8] Experimental prototype of the proposed inverter.

![Fig. 9] Circuit diagram of the power circuit of the prototype.

### Table 4  Components used in the prototype.

<table>
<thead>
<tr>
<th>Name</th>
<th>Detail</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>GaN-HEMT S1, S2</td>
<td>GS66516B</td>
<td></td>
</tr>
<tr>
<td>Reverse-parallel SBD D1, D2</td>
<td>C3D03065E</td>
<td></td>
</tr>
<tr>
<td>Gate driver IC</td>
<td>LM5114B (6-Pin SOT-23 package)</td>
<td></td>
</tr>
<tr>
<td>Input decoupling ceramic capacitor ( C_{in} )</td>
<td>GCM32D7U2J103XJ01; 3 parallel</td>
<td>0.027µF at 13.56MHz</td>
</tr>
<tr>
<td>Input film capacitor ( C_{film} )</td>
<td>CDE715P909V104J</td>
<td>0.1µF at DC</td>
</tr>
<tr>
<td>Air core coil inductor ( L ) in the L-network</td>
<td>Wire: #2.24mm Wire: #2.24mm</td>
<td>0.179µH at 13.56MHz</td>
</tr>
<tr>
<td>Toroidal coil resonant inductor ( L_s )</td>
<td>Core: T106-2 Wire: #2.24mm Number of turns: 3</td>
<td>1.0µH at 13.56MHz</td>
</tr>
<tr>
<td>Parallel capacitor ( C ) in the L-network</td>
<td>GRM32B7U23D3F101JW31; 3 parallel GRM42A7U3F050DW01; 2 parallel</td>
<td>880.7µF at 13.56MHz</td>
</tr>
<tr>
<td>Resonant capacitor ( C_s )</td>
<td>GRM42A7U3F330J104J</td>
<td>138pF at 13.56MHz</td>
</tr>
</tbody>
</table>

### Table 5  Parameters in the experimental prototype.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Load resistance at 13.56MHz (Ω)</td>
<td>( R_{load} )</td>
<td>50.37</td>
</tr>
<tr>
<td>Input resistance of the L-S network (Ω)</td>
<td>( r_0 )</td>
<td>2.92</td>
</tr>
<tr>
<td>Input reactance of the L-S network (Ω)</td>
<td>( x_0 )</td>
<td>2.73</td>
</tr>
</tbody>
</table>

#### 5.2 13.56MHz Gate Driver Circuit

Fig. 10 shows the schematic of the gate driver circuit for driving GaN-HEMTs at 13.56MHz. High-speed switching of the GaN-HEMT is achieved by using LM5114B gate driver IC. Two external gate resistors 1.8Ω 0.5W ERJP06J1R8V and 2.2Ω 0.5W ERJP06J2R2V are used for gate-charging drive path and gate-discharging drive path, respectively.
Resistances of these resistors are important. At turn-on, the gate current flows into the gate-drain capacitance \( C_{\text{RSS}} \) following the charging of the gate-source capacitance \( C_{\text{ISS}} \), so ringing is unlikely to occur on gate-source voltage \( v_{gs} \). However, rising of \( v_{gs} \) slows down. It was necessary to suppress this slowdown as much as possible, and 1.8Ω was selected for this purpose. At turn-off, the drain current flows into \( C_{\text{RSS}} \), rapidly pushing out the \( C_{\text{RSS}} \) charge to the gate, and \( v_{gs} \) falls sharply. \( v_{gs} \) undershoot and \( v_{gs} \) ringing may occur. Falling speed of \( v_{gs} \) should be slowed down slightly so that \( v_{gs} \) does not exceed the gate-source negative breakdown voltage of GaN-HEMT, and at the same time the turn-off should not be too slow to avoid slowdown of switching speed. Therefore, 2.2Ω was selected. The other purpose of these gate resistor is to protect the gate driver IC from over-heating.

The dead time generator block consists a NAND logic IC RD74LVC00BF-E and two RC transient circuits, and it adds 7ns dead time in each driving signal. The ISO721MD high-speed isolator transmits isolated signal to the high-side driver circuit which is based on different potential. LM5114B and the secondary side of ISO721MD are powered by an isolated DC-DC power supplies not shown in Fig. 10. Common mode choke coil DLW43SH220XK2L is connected to the input of each DC-DC power supply to prevent malfunction due to high frequency noise from the high-side GaN-HEMT switch. This common mode choke coil has a common mode impedance of 1kΩ at 15MHz. By means of these circuits, voltage 6V for turn-on and -3.3V for turn-off are applied to gate to source of each GaN-HEMT alternately.

In addition, it is important to properly select the power supply bypass capacitor for the LM5114B in order to inject electric charge into the LM5114B instantly. It is necessary to use a bypass capacitor with a small equivalent series resistance (ESR) to prevent voltage dropping. C2012X5R1V-106K085AC 10µF ceramic capacitors with ESR of 10mΩ at 13.56MHz is used for this purpose in the prototype. These capacitors are connected to LM5114B as shown in Fig. 10.

5.3 Passive L-S Network

In the proposed L-S network, a significantly large current flows only in the impedance converter L-network. Therefore, it is important to implement the L-network with low loss in order to improve the efficiency of the entire circuit. The L-network inductor was designed as air-core thick helical coil as described in Table. 4 to meet this requirement. The material of this coil wire is copper with 99.93% purity. ESR of this inductor was measured as 8mΩ at 13.56MHz. Parasitic parameters of PCB are also included in these measured values. The parallel capacitor \( C \) is composed of a plurality of capacitors connected in parallel in order to reduce the overall ESR. The low ESR of the L-network makes the entire inverter circuit highly efficient.

The input impedance of the entire L-S network is measured as 2.92±/2.73Ω at 13.56MHz for an oil-cooled load with 50.37Ω. Fig. 11 shows the measured frequency characteristics of impedance, resistance \( r_{\text{in}} \) and reactance \( x_{\text{in}} \) of the L-network connected to a 50Ω chip resistor without the series resonator. Fig. 12 shows the measured input impedance of the entire L-S network including the L-network, the series resonator, and the 50.37Ω load. The cause of the slight difference of the input impedances at 13.56MHz between Fig. 11 and Fig. 12 is parallel parasitic capacitance as tens of pF between the series resonator and the PCB ground plane.

The series resonator is designed independently of the L-network. Unlike in the L-network, its ESR requirements can be loose due to the smaller current. The series resonator is specialized as harmonics filter by giving a high loaded quality-factor with high inductance. Self-inductance \( L_s \) and ESR of the resonant inductor were measured as 1.003μH and 153mΩ at 13.56MHz, respectively.

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**Fig. 10** Circuit diagram of the 13.56MHz gate driver circuit.

**Fig. 11** Measured frequency characteristics of input impedance of the L-network with 50Ω resistor.

**Fig. 12** Measured frequency characteristics of input impedance of the entire L-S network with the 50.37Ω load.
5.4 PCB Layout

The prototype of the proposed inverter is shown in Fig. 13. The PCB base material is FR4, and thickness of FR4 and copper layers are 1.2mm and 150µm. The PCB wiring pattern for the half-bridge configuration is designed as short and wide to reduce the parasitic impedances. For the same purpose, the ground return-path to the DC input capacitors is allocated directly back side of the half-bridge configuration. It is important to reduce the gate wiring inductance to suppress $v_{gs}$ ringing. Each length of gate-charging and gate-discharging drive path-way is 6.8mm which is short enough. These path-way include external gate resistors.

Unlike the low-side, the high-side is electrically isolated from the circuit ground by the PCB insulation material. Due to this PCB construction, it is inevitable that the heat dissipation ability for cooling the high-side switch will decrease. This problem is mentioned in the later section 5.6 also, and it remains as a future work.

5.5 Input Capacitive Loop Suitable for 13.56MHz

The purpose of this section is to describe the method to reduce generation of voltage noise in GaN-HEMTs without using loss-causing snubber resistors such as [32]–[34]. The authors attach ceramic capacitors and a film capacitor to the half-bridge configuration as decoupling capacitors $C_{dc}$ and an input smoothing capacitor $C_{film}$, respectively as shown in Fig. 9. The important point that the authors given to this architecture is that the total capacitor loop has capacitive impedance at 13.56MHz, not inductive. This scheme has the effect of bringing the switching waveform of the experimental prototype closer to that of the theoretical operation. According to the simulation result of Fig. 6, there are rapid-changes in current across $C_{DSS}$, $C_{SBD}$, and SBDs. The drain current changing is also relatively fast due to high frequency of 13.56MHz. Therefore, it is preferable to provide capacitive impedance in order to supply charges quickly to the half-bridge configuration.

The experimental prototype achieves the above requirements by the capacitive impedance of the DC decoupling loop of the half-bridge switch. Three parallel GCM32D7U2J103JX01 0.01µF U2J ceramic capacitors are used as the decoupling capacitor $C_{dc}$. The capacitive impedance of the loop is confirmed by the measurement as shown in Fig. 14. The measured capacitance of this loop is 79.71nF at 13.56MHz.

A CDE715P600V104J 0.1 µF audio film capacitor is also connected to the DC bus in parallel as an input smoothing capacitor $C_{film}$. Though this film capacitor has relatively small ESR at 13.56MHz than that of other similar products, its impedance is inductive at 13.56MHz due to parasitic inductance. Then, the impedance phase-angle of the DC decoupling loop is measured. Fig. 15 shows the setup for the measurement. The high-side switch is shorted by a small copper piece and the low-side switch is opened as shown in Fig. 15, and the loop is measured at the position of low-side switch by IM7581 impedance analyzer.

The measured results with and without film capacitor is shown in Fig. 14. From these results, it was found that capacitive impedance is secured at 13.56MHz even if the inductive film capacitor is used with ceramic capacitors. The measured capacitance of the loop is 61.95nF at 13.56MHz with the film capacitor. This characteristic will be very convenient in the practical use having DC bus capacitors.

![Fig. 13 PCB layout of the prototype inverter including the gate drivers.](image)

![Fig. 14 Measured frequency characteristics of the impedance phase angle of the half-bridge decoupling loop.](image)

![Fig. 15 Setup for measuring the impedance of the half-bridge configuration including the input capacitors.](image)
5.6 Thermal Components and Heat Dissipation

Because GS66516B GaN-HEMT is ‘bottom-cooled’ device, a copper heat spreader is installed back-side of the PCB half-bridge configuration in the prototype inverter. In addition to that, an aluminum heat sink is attached under the heat spreader. The size of the heat sink is 150 x 69 x 37mm, and it is cooled by air.

It is designed that the low-side GaN-HEMT S2 is efficiently cooled by making good thermal connections between its source pad and the heat spreader under the PCB by means of metal via-holes in the PCB. Whereas, the high-side GaN-HEMT S1 cannot be thermally connected to the heat spreader because the electric potential of its source pad is different from the circuit ground potential of the heat spreader. Instead, the PCB pattern of half-bridge path is widened, and conductor layer of the PCB is thickened to improve heat dissipation and conductor layer of the PCB is thickened to improve heat dissipation even a little.

5.7 Probing Method on Measurements

Probing techniques are very important because the experimental prototype is operated in high frequency and high-speed switching. The ground spring is used for probing low-side gate-source voltage $v_{gs2}$ as shown in Fig. 16a to reduce the parasitic impedance on probing. Low-side drain-source voltage $v_{ds2}$ and output voltage $v_{out}$ are measured by fixed probe on the PCB as shown in Fig. 16a and 16b to minimize the parasitic impedance, especially a grounding impedance. In the latter method, the terminals of the probe are fixed on the PCB by means of two surface mounted signal check terminals as shown in Fig. 16a and 16b.

![probing](a) ![probing](b)

Fig. 16 Probing methods for measuring gate-source and drain-source voltages (a) and output voltage (b).

### 6. Experimental Results

The prototype of the proposed inverter was tested to verify the circuit operations, high power and sinusoidal output wave with low-distortions at 13.56MHz. DC voltage 105.6V was applied to the inverter input, and waveforms in the inverter were measured. Fig. 17 shows the voltage waveforms of the proposed inverter measured by using a wavesurfer-3054 oscilloscope having a frequency bandwidth of 500MHz with the sampling speed of 2GS/s and PP020 voltage probes having a frequency bandwidth of 500MHz. Input DC current and input power were measured as 4.49A and 474.1W, respectively. The measured amplitude of the output sine wave voltage was 218.0V at 50.37Ω load. Therefore, the effective output voltage was 154.1V. The output power is 471.4W, and the conversion efficiency of the power circuit is 99.4% by dividing the output power by the input power. The measured input voltage, current, and power of the entire gate driver circuit are 12.0V, 0.3A, and 3.6W, respectively. Therefore, the entire inverter efficiency including the gate driver circuit is 98.7%. There are no switching surges or spikes on the drain-source voltage $v_{ds2}$ waveform as shown in Fig. 17. The output voltage $v_{out}$ is clear sinusoidal wave.

![Measured waveforms of the proposed inverter at 471.4W](image)

Note that, in this experiment, the input power was obtained as a product of time-averaged values of the input voltage and the input current measured by the voltage probe PP020 and the current probe CP031A which has a frequency bandwidth of 100MHz. Since the input capacitors described in Section 5.5 are implemented, the input voltage and current are almost DC. Therefore, the phase error between the voltage probe and the current probe does not matter. Since it is DC power, there are no problems due to the frequency band of the oscilloscope and probes.

Whereas, the value of the RF output power was obtained by probing only $v_{out}$. Although the power measurement method based on current and voltage is familiar in low frequency circuits, the phase error between the voltage probe and the current probe cannot be ignored in MHz-frequency high power circuit. Therefore, the authors measured $v_{out}$ by using only the PP020 voltage probe and the oscilloscope and obtained the time-averaged value of the output power by dividing the squared value of the effective voltage of $v_{out}$ by the load resistance $R_{load}$. Hence, the problem of phase error was avoided. $R_{load}$ was 50.37Ω measured by the impedance analyzer IM7581 having a frequency band of 100kHz to 300MHz and measurement accuracy of 99.28%.

Fig. 18 shows the measured waveforms of the current $i_{hb}$ outputted from midpoint of the half-bridge switch. $i_{hb}$ is measured in the L-network inductor by using a de-skewed Rogowski probe. There is a time difference of 15.2ns from the start of rising of $v_{ds2}$ to the zero-crossing of $i_{hb}$. It means that the switching under the inductive impedance is achieved.
for ZVS operation. The drain current itself is not measured in this prototype because inserting a current probe in drain-path requires an additional jumper wire which will increase inductance of the half-bridge decoupling loop.

Fig. 19 shows the thermography of operating prototype in thermal equilibrium state at outputting 471.4W, 20 minutes after the start of operation. The temperature of the low-side GaN-HEMT is low enough as 35°C. However, the temperature of the high-side GaN-HEMT is 71°C. Compared with the low-side GaN-HEMT, it is considered that heat is trapped in the high-side GaN-HEMT due to thermal insulation by the PCB as described in Section 5.6. Although GaN-HEMTs have low power loss and low heat generation, its temperature will surely rise if heat cannot be dissipated. Measured temperature of each component in thermal equilibrium state is listed in Table 6. Though the high temperature of the high-side GaN-HEMT interferes with higher power operation in the present prototype, this problem can be solved by using heat-conductive electrical-insulation material. In the future work, new prototype for higher power will be implemented by improving the heat dissipation ability for the high-side GaN-HEMT.

**Table 6** Measured temperature of each component at 471.4W.

<table>
<thead>
<tr>
<th>Component</th>
<th>Temperature (°C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>High-side gate driver IC</td>
<td>65</td>
</tr>
<tr>
<td>Low-side gate driver IC</td>
<td>62</td>
</tr>
<tr>
<td>High-side common mode choke coil</td>
<td>37</td>
</tr>
<tr>
<td>Low-side common mode choke coil</td>
<td>30</td>
</tr>
<tr>
<td>High-side GaN-HEMT S1</td>
<td>71</td>
</tr>
<tr>
<td>Low-side GaN-HEMT S2</td>
<td>35</td>
</tr>
<tr>
<td>L-network parallel capacitors C</td>
<td>29</td>
</tr>
<tr>
<td>Series resonant capacitors Cs</td>
<td>28</td>
</tr>
<tr>
<td>Series resonant inductor Ls</td>
<td>26</td>
</tr>
<tr>
<td>Aluminum heat sink</td>
<td>24</td>
</tr>
</tbody>
</table>

7. Conclusion

In this study, the use of half-bridge topology as MHz-frequency inverter was discussed from the point of view of protecting GaN-HEMTs against overvoltage. The novel topology has been proposed to achieve both high power and low distortion under low drain-source voltage. The process of individual specialized design of each component to achieve the requirements of the entire circuit was presented. The 3kW output to 50Ω at 13.56MHz with drain-source voltage of 280V was designed theoretically and verified by computer simulations. Experimental results verified the effectiveness of the proposed topology. High conversion efficiency as 99.4% was achieved at output power of 471.4W. The proposed topology is suitable for GaN-HEMTs and possible to contribute to improvements of the MHz-frequency ISM bands applications.

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References


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