A Hardware Oriented Approximate Convex Hull Algorithm and its FPGA Implementation*

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SUMMARY The convex hull is the minimum convex surrounding a given set of points. Since the process of finding convex hulls has various practical application fields including embedded real-time systems, efficient acceleration of convex hull algorithms is an important problem in computer geometry. In this paper, we discuss an FPGA acceleration approach to address this problem. In order to compute the convex hull of an unsorted point set, it is necessary to store all the points during the computation, and thus the capacity of on-chip memory is likely to be a major constraint for efficient FPGA implementation. On the other hand, approximate convex hulls are often sufficient for practical applications. Therefore, we propose a hardware oriented approximate convex hull algorithm, which can process the input points as a stream without storing all points in the memory. We also propose some computation reduction techniques for efficient FPGA implementation. Then, we present FPGA implementation of the proposed algorithm, which is parallelized both in temporal and spatial domains, and evaluate its effectiveness in terms of performance and accuracy. As a result, we demonstrated 11 to 30 times faster performance compared to the widely-used convex hull software library Qhull. In addition, accuracy assessment revealed that the maximum approximation error normalized to the diameters of point sets was 0.038%, which was reasonably small for practical use cases.

key words: convex hull, hardware algorithm, FPGA, approximated algorithm

1. Introduction

Given a point set \( P \), the minimum convex that includes all the points in \( P \) is called the convex hull of \( P \). For example, for point sets defined on a two dimensional (2D) planar space, the convex hull of \( P \) becomes the convex polygon whose vertices are a subset of \( P \) as illustrated in Fig. 1. A convex hull problem, whose purpose is to find the convex hull \( CH(P) \) of a given point set \( P \), has various practical applications [2], and thus its high speed algorithms and implementation have been widely addressed in the field of computational geometry.

Qhull [3] is one of the most popular software libraries for computing convex hulls. The main algorithm used in the Qhull library is called Quickhull [4], [5]. Mei proposed a GPU-accelerated high-speed 2D convex hull algorithm called CudaChain [6]. CudaChain firstly reduces interior points of a given point set to form a simple polygon. This step is parallelly performed on a GPU. Then, the convex hull of the simplified polygon is computed with Melkman’s algorithm [7] on a CPU. Performance evaluation revealed that CudaChain with GT640 and GTX660M GPUs outperforms Qhull by a factor of 5 to 6 for a 20M-point set. Srungarapu et al. implemented the Quickhull algorithm on a GTX280 GPU and achieved 14 times speedup to Qhull [8]. Srikanth et al. also parallelized the Quickhull algorithm and evaluated the performance on a GTX280 GPU as well as a Cell Broadband Engine [9]. The GPU implementation achieved approximately 15 times speedup to Quickhull implementation on a CPU, while Cell Broadband Engine implementation obtained 4 to 5 times performance compared to the main processor execution. Tzeng et al. implemented a general GPU framework for divide-and-conquer algorithms and applied it to accelerate 2D and 3D convex hull computations [10]. Compared to Qhull implementation, they demonstrated more than 10 times acceleration.

Aiming at effective real-time convex hull calculation, Kemmotsu et al. proposed an FPGA-based parallel approach for convex hull computing for points in 2D images [11]. The basis of this approach is Andrew’s Monotone Chain [12], which needs the input points to be sorted in advance as a pre-processing step. Kemmotsu’s approach eliminates the pre-processing step from the implementation by limiting application domains to image processing, in which input points are always given in a raster scan manner. They also proposed to parallelly compute the upper hull and the lower hull. The final result is obtained by combining them. However, the approach is not suitable for general systems that need to handle unsorted input points.

In typical convex hull algorithms for unsorted point sets, such as Graham’s scan [13], Andrew’s Monotone Chain [12], and Quickhull [4], entire input points need to be stored and...
available in memory before starting computation, which imposes a challenge for FPGA implementation. Since the capacity of on-chip memory of FPGAs is limited, the use of external memory is required to avoid size (the number of points) limitation of solvable problems. However, this approach will significantly reduce the advantage of FPGAs, in terms of both performance and power efficiency. For FPGAs, online algorithms that can process the input in a point-by-point manner are more preferable.

Fortunately, convex hulls are often used to roughly grab abstract object shapes in applications such as collision detection and path planning, where computation of the exact convex hulls is not necessarily needed. For such application domains, approximate convex hull computing algorithms [14]–[17] are acceptable. In this paper, we propose an online approximate convex hull algorithm for unsorted point sets and present its FPGA implementation. This algorithm is hardware oriented, in a sense that input points can be processed in a pipelined manner without storing all the points in memory. As far as the authors’ knowledge, FPGA implementation of such online approximate convex hull algorithms has not been reported so far.

The rest of the paper is organized as follows. The proposed algorithm is described in Section 2, and the FPGA implementation is shown in Section 3. In Section 4, we evaluate the implementation by comparing the performance to related work [6] and the software library Qhull [3]. Finally, Section 5 concludes this paper.

2. Algorithm

Let $\theta$ be an angle between a unit vector $v \in \mathbb{R}^2$ and a position vector $P \in \mathbb{R}^2$. Let us consider an inner product map $d : \mathbb{R}^2 \to \mathbb{R}$ such that:

$$d(P) \equiv v^T P = ||v|| ||P|| \cos \theta = ||P|| \cos \theta \tag{1}$$

where $\theta$ is the angle between the two vectors $P$ and $v$. Let $\ell$ be the line with the direction vector $v$ passing through the origin. As depicted in Fig. 2, $d(P)$ can be interpreted as the signed distance between the origin and the point $P'$, which is the projection of point $P$ on the line $\ell$.

Let us consider that all the points in a given point set $P$ are projected onto a line $\ell$. If a projected point becomes one of the end points on the line $\ell$, the corresponding original point is one of the vertices of the convex hull $CH(P)$ as shown in Fig. 3 and Fig. 4. Therefore, the vertices of $CH(P)$ can be obtained by finding the points $P \in P$ which have the maximum or minimum value of $d(P)$, by rotating the unit vector $v$. Here, we call $v$ a scan vector. Although ideally the scan vector should be continuously rotated to scan the 2D plane, we need to discretize the algorithm using a small step angle for implementation. By rotating the scan vector in the counterclockwise direction, the vertices of the convex hull can be obtained in a counterclockwise order as illustrated in Fig. 5.

While this principle is also shared by other approximate convex hull algorithms such as [14] and [17], we
introduce a computation reduction technique for FPGA implementation as follows. A naive calculation of one inner product in Eq. (1) requires two multiplications. Utilizing symmetry, however, four inner products can be computed by two multiplications. With a polar coordinates system, a unit product in Eq. (1) requires two multiplications. Utilizing (green nodes). Their original points form the vertices of the convex hull (green nodes).

Here, let us consider the following four symmetric vectors:

$$\mathbf{v}_0 = \mathbf{v}(\theta), \quad \mathbf{v}_1 = \mathbf{v}\left(\frac{\pi}{2} - \theta\right), \quad \mathbf{v}_2 = \mathbf{v}\left(\theta + \frac{\pi}{2}\right),$$

$$\mathbf{v}_3 = \mathbf{v}(\pi - \theta)$$

where \( \theta \in \left[0, \frac{\pi}{4}\right] \). The inner products between point \( \mathbf{P} = (p_x, p_y)^T \) and these vectors can be expressed as:

$$d_0(\mathbf{P}) \equiv \mathbf{v}_0^T \mathbf{P} = p_x \cos \theta + p_y \sin \theta$$
$$d_1(\mathbf{P}) \equiv \mathbf{v}_1^T \mathbf{P} = p_x \sin \theta + p_y \cos \theta$$
$$d_2(\mathbf{P}) \equiv \mathbf{v}_2^T \mathbf{P} = -p_x \sin \theta + p_y \cos \theta$$
$$d_3(\mathbf{P}) \equiv \mathbf{v}_3^T \mathbf{P} = -p_x \cos \theta + p_y \sin \theta.$$

Dividing the both sides of Eq. (4) by \( \cos \theta \), we get:

$$d'_0(\mathbf{P}) = p_x + p_y \tan \theta$$
$$d'_1(\mathbf{P}) = p_x \tan \theta + p_y$$
$$d'_2(\mathbf{P}) = -p_x \tan \theta + p_y$$
$$d'_3(\mathbf{P}) = -p_x + p_y \tan \theta$$

where \( d'_i(\mathbf{P}) \equiv \frac{d_i(\mathbf{P})}{\cos \theta} \). Since \( \cos \theta > 0 \) for \( \theta \in \left[0, \frac{\pi}{4}\right] \),

$$d_i(\mathbf{P}_0) \leq d_i(\mathbf{P}_1) \iff d'_i(\mathbf{P}_0) \leq d'_i(\mathbf{P}_1)$$

for any pair of points \( \mathbf{P}_0 \) and \( \mathbf{P}_1 \). Therefore, we can use \( d'_i(\mathbf{P}) \) in stead of \( d_i(\mathbf{P}) \) for judgment of end points. By pre-calculating the value of \( \tan \theta \), the four inner products in Eq. (5) can be computed with two multiplications, that is, \( p_x \tan \theta \) and \( p_y \tan \theta \).

The proposed approximate convex hull algorithm is described in Algorithm 1. Here, \( n \) and \( s \) are the size of a given point set and the number of scan vectors in \([0, \frac{\pi}{4}]\), respectively. In this algorithm, a circle is divided into eight sectors as shown in Fig. 6, and the point numbers (IDs) on the convex hull are pushed into each stack \( N_0, N_1, \ldots, N_7 \) in a scanned order. Since the computation for one scan takes \( O(n) \), the time complexity for sequential execution of this algorithm is \( O(ns) \). If we make \( s \) a small value, the execution time will be reduced, but the approximation error will increase.

**Algorithm 1: Approximate convex hull algorithm**

**Input:** \( \mathcal{P} = \{P_0, P_1, \ldots, P_{n-1}\} \): Point set

\( n \): number of scan vectors in \([0, \frac{\pi}{4}]\)

**Output:** Array of point ID s for convex hull vertices in counterclockwise

**Data Structure:** \( N_0, N_1, \ldots, N_7 \): Stacks

1. for \( i = 1, \ldots, n-1 \) do
2. \( P_i := P_{i-1} - P_0; \)
3. end for
4. for \( i = 0, \ldots, s-1 \) do
5. \( \theta := \frac{i \pi}{4s}; \)
6. for \( k = 0, 1, 2, 3 \) do
7. \( n_k = \arg \max d'_k(P_j); \)
8. \( n_{k+4} = \arg \min d'_k(P_j); \)
9. end for
10. for \( k = 0, \ldots, 7 \) do
11. if \( i = 0 \) or \( n_k \neq N_k.top() \) then
12. \( N_k.push(n_k); \)
13. end if
14. end for
15. end for
16. \( N_{2k+1}.reverse(); \)
17. end for
18. \( return \) unite(\( N_0, \ldots, N_7 \))
3. Implementation

We designed pipeline-based custom hardware for the proposed approximate convex hull algorithm. Since the calculation for each scan vector is independent, we prepared as many calculation modules as the number of scan vectors to extract parallelism. The overall diagram of the circuit is as shown in Fig. 7. The roles of each signal and parameter are summarized in Table 1. The implemented circuit receives information for one point (point ID and \(x, y\) coordinates) every clock cycle. The circuit starts output of the point IDs for the vertices of the calculated convex hull one by one each cycle, several clock cycles after whole point information has been given.

The horizontally arranged rectangles in Fig. 7 show INNER_MINMAX circuits, for each of which a unique scan vector \(v\) is assigned. This circuit calculates the inner products between the input point and the four symmetric vectors \(v_0, \ldots, v_3\), and holds the maximum and minimum values as well as the corresponding point IDs. After the input of the point set and the calculation of the INNER_MINMAX circuit are completed, the approximate convex hull is obtained by outputting the point IDs in a counterclockwise order while eliminating duplication.

The \(x, y\) coordinate values of the first input point \(P_0\) are stored in \(x_0\) and \(y_0\) registers depicted in Fig. 7. The coordinates of the subsequent input points are transformed so that \(P_0\) is the origin by subtracting \(x_0\) and \(y_0\). Each INNER_MINMAX circuit reads \(n, x, y\) and updates the provisional maximum and minimum points by calculating the inner products. The signal “in_en” is an input enable signal, thus the register values are not updated when this port is deasserted. The signal “in_complete” represents the completion of the input stream. Once this port is asserted, the subsequent input signals are just ignored without being stored in the registers.

The update of the INNER_MINMAX circuit is finished several clock cycles after “in_complete” becomes 1, and output of the result starts. After output starts, “out_flag” goes to 1. Meanwhile, another flag “store_bram” becomes 1 for \((s + 1)\) clock cycles. Then the point IDs in the region \(N_0 (\theta \in [0, \frac{\pi}{4}])\) are outputted from “out_n” in the counterclockwise order, while the point IDs in \(N_1 \sim N_7\) are stored in BRAM, eliminating duplicates. Note that the point IDs in \(N_1, N_3, N_5,\) and \(N_7\) are stored from the \(\theta = \frac{\pi}{4}\) side, so that they are obtained in the counterclockwise order.

The output of the IDs from \(N_0\) is completed as soon as “store_bram” becomes 0, and the point IDs stored in BRAM are outputted from “out_n” in the order of \(N_1 \sim N_7\) thereafter. Two clock cycles after the completion of \(N_7\) output, “out_complete” goes to 1 to show the completion of the output.

For each INNER_MINMAX circuit,

\[ \mathbf{v} = (v_x, v_y) = \left(2^w, [2^w \cdot \tan \theta]\right)^T \]  \hspace{1cm} (7)

is assigned as a scan vector. Since the norm of \(\mathbf{v}\) can be changed to any value provided that the orientation is kept, both \(v_x\) and \(v_y\) are right-shifted so that the LSB of \(v_x\) becomes 1, aiming at hardware resource reduction. When “out_flag” is 0, the circuit receives input points from “in_n”, “in_x”, and “in_y”, and updates the maximum and minimum values of the inner products and the point IDs as Fig. 8 shows. When “out_flag” is 1, the point IDs given from the outside are stored in the registers \((n_0, \ldots, n_7)\), which are used to store point IDs in Fig. 8, in order to form the shift register shown in Fig. 7.
In this architecture, it takes \( (n + 4) \) clock cycles to process all the input points with INNER_MINMAX circuits. Since the maximum number of output points is \( 8s \), which corresponds to the situation there is no duplication in the detected convex hull vertices, at most it takes \( (8s + 2) \) clock cycles to output the results. Therefore, the theoretical execution time \( T \) can be expressed as

\[
T \leq \frac{n + 8s + 6}{F_{\text{max}}}
\]

(8)

where \( F_{\text{max}} \) is the maximum clock frequency of the system. Thus, the time complexity of the FPGA execution is \( O(n + s) \), in contrast to the time complexity for sequential execution of \( O(ns) \).

Unlike to other convex hull algorithms, the proposed method does not adopt preprocessing to decimate input points. In general, the time complexity of the exact (unapproximate) convex hull algorithms is \( O(n \log n) \). Thus, it is reasonable to perform preprocessing in \( O(n) \) to reduce the number of points to be processed. On the other hand, the proposed approach calculates an approximated convex hull in \( O(n + s) \). Therefore, decimation of input points is not considered for this approach.

4. Evaluation

The designed hardware was evaluated targeting on a Xilinx Virtex UltraScale FPGA (xcvu95-fiva2104-2-e-es2). For logic synthesis and mapping, Xilinx Vivado 2018.3 was used. For simulation, Cadence Xcelium 18.9 was used. For evaluation of execution time and approximation errors, the benchmark point sets used in the related work [6] were used. The benchmark sets consist of three groups: rbox, circle, and model. The rbox group contains point sets generated using Qhull’s rbox, and their sizes (the number of points) are 0.1M, 0.2M, 0.5M, 1M, 2M, 5M, 10M, and 20M. The circle group contains point sets randomly generated within the unit circle, and their sizes are the same as those for the rbox group. The model group contains point sets obtained by projecting the vertices of 3D models onto the XY plane. The 3D models and their sizes are shown in Table 2. These models were obtained from the Stanford 3D Scan Repository [18] and the GIT Large Geometry Models Archive [19].

For the circuit parameters shown in Table 1, we evaluated four types of \( s = 50, 150, 250, \) and 350 (\( W_s = \lceil \log_2 s \rceil \)). \( W_s \) is set to 25 bits so that the maximum size of evaluation point sets (20M) can be addressed. Both \( W_s \) and \( W_r \) are set to 32 bits. At each rising clock edge, one point ID and corresponding real type \( xy \) coordinate values are read from the input point set. The coordinate values are multiplied by \( 2^{30} \) and the integer values are given to the circuit by truncating the fractional part.

For comparison, we evaluated the performance of software execution using the Qhull library (2019) on a PC with the following environments:

- CPU: Intel i9-9900K (3.6GHz), Memory: 16GB, OS: CentOS Linux 7.6.1810

We also compare the performance with GPU implementation described in [6], where the following two computational environments were used:

- GPU: GT640, CPU: Intel i5-3470, Memory: 8GB, OS: Window 7 Pro
- GPU: GTX660M, CPU: Intel i7-3610QM, Memory: 6GB, OS: Window 7 Pro

For the execution time of Qhull, the average of 18 runs was used. The execution time for the FPGA implementation was obtained by dividing the number of clock cycles from the start of input to the end of output in HDL simulation with the maximum operating frequency obtained by Vivado STA.

To evaluate accuracy of the proposed approximate convex hull algorithm, we utilized several metrics as follows.

Let \( CH(P) \) be the convex hull obtained by Qhull for the point set \( P \), and \( CH'(P) \) be the approximate convex hull obtained by this implementation. Let \( V = \{ v_0, v_1, \ldots, v_{n-1} \} \) and \( V' = \{ v'_0, v'_1, \ldots, v'_{n-1} \} \) be the vertices of the convex hull \( CH(P) \) and \( CH'(P) \), respectively. The order of both vertex sets is counterclockwise. The boundaries \( \partial CH(P) \) of \( CH(P) \) and \( \partial CH'(P) \) of \( CH'(P) \) are polygons that connect \( V \) an \( V' \), respectively. We consider an approximation evaluation metric \( r \), which is defined as the ratio of the number of points that belong to the vertices of the approximate convex hull to the vertices of the exact convex hull, that is,

\[
r = \frac{\| \{ v \in V | v \in V' \} \|}{\| V \|}.
\]

(9)

The higher the value of \( r \), the better approximation. Note that we regard the convex hull obtained by Qhull as the exact convex hull, in this evaluation.

However, this metric alone would not be enough to assess the approximation quality. As an extreme example, if only one point of the approximate convex hull is wrong and that point is far away from the exact convex hull as shown in Fig. 9, \( r \) takes a large value but it cannot be said to be good approximation. Therefore, we also evaluated the value \( \mu \), which is the maximum value of the shortest distances among the vertices and boundaries between the exact convex hull and the approximate hull as shown in Fig. 10. In addition, to remove the effect of size of convex hulls, the value of \( \mu \) is normalized to the diameter of the point set \( P \):

\[
\mu = \max_{v \in V} \left( \frac{\max_{v' \in V'} d(v, \partial CH'(P))}{\max_{v' \in V'} d(v', \partial CH(P))} \right) / \text{diam}(P)
\]

(10)
4.1 Resource usage and execution performance

The resource usage and the maximum operating frequency (Fmax) of this implementation are listed in Table 3. When \( s = 50 \), the resource usage was small and the maximum operating frequency was close to 300MHz. When \( s = 150, 250, \) and 350, the maximum operating frequency was about 180MHz, which was 100MHz or more lower than that of \( s = 50 \). This is because the increase in the number of INNER_MINMAX circuits makes wiring congestion on the FPGA, resulting in an increase in wiring delays. Each time \( s \) was increased by 100, LUT utilization and FF utilization were increased by about 12 pt and 8 pt, respectively. Assuming a linear relationship between resource usage and \( s \), the target FPGA (Virtex UltraScale xcvu095-ffva2104-2-e-es2) will be able to configure the system up to \( s = 750 \).

Since the size of each stack is \( s + 1 \), the required memory capacity is \( W_n \times (s + 1) \) bits. Here, if \( W_n = 25 \) and \( s = 350 \), the required capacity becomes 8,775 bits, which corresponds to half of 0.5 BRAM (in this device, one BRAM can be utilized as two memory module each contains 18,000 bits). Therefore, as shown in Table 3, the total amount of BRAM remained at 0.5 \( \times 7 = 3.5 \) regardless of \( s \). This does not change even when \( s \) reaches 700, so BRAM usage does not limit the solvable problem size on this system.

Fig. 11 shows the speedup ratios for CudaChain and our implementation to Qhull execution. Table 4 represents the execution times for implementations shown Fig. 11. When \( s = 50 \), the maximum operating frequency was high, and thus it was approximately 1.5 times faster than the designs with \( s = 150, 250, \) and 350. When \( s = 150, 250, \) and 350, there was almost no difference in terms of the maximum operating frequency and the execution time. This implementation is 18 to 30 times faster when \( s = 50 \), and 11 to 19 times faster when \( s = 150, 250, \) and 350 compared to Qhull. Compared to the implementation for \( s = 50 \), the performance was dropped when \( s = 150, 250 \) and 350. This is due to the FPGA implementation. An increase in \( s \) also increases the complexity of the FPGA circuit, resulting in the slower clock frequency.

Table 3 Resource usage and maximum operating frequency.

<table>
<thead>
<tr>
<th>( s )</th>
<th>( W_n )</th>
<th>LUT [%]</th>
<th>FF [%]</th>
<th>BRAM [%]</th>
<th>Fmax(MHz)</th>
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<tbody>
<tr>
<td>50</td>
<td>6</td>
<td>22.6</td>
<td>3.04</td>
<td>3.5</td>
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<td>150</td>
<td>8</td>
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<td>17.31</td>
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<td>250</td>
<td>8</td>
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<td>18.47</td>
<td>189.29</td>
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<tr>
<td>350</td>
<td>9</td>
<td>225.054</td>
<td>41.86</td>
<td>26.36</td>
<td>188.47</td>
</tr>
</tbody>
</table>

Fig. 11 Speedup ratios to Qhull execution.
as shown in Table 3. In addition, compared to CudaChain, it was more than 5 times faster when \( s = 50 \) and more than 3 times faster when \( s = 150, 250, \) and \( 350 \). Related work [8] achieved up to 14 times speedup to Qhull, and related work [10] achieved more than 10 times faster performance than Qhull. Since the point sets and Qhull versions used for evaluation differ from these GPU implementations in the literature, precise comparisons cannot be made, but at least we achieved higher performance than these GPU implementations.

### 4.2 Execution efficiency

Table 5 shows power consumption, execution time, total energy, and energy efficiency for for this method and GPU implementation in related work. Here, the energy efficiency was defined as the number of points processed per unit energy consumption. Our design was implemented on a Xilinx VCU108 evaluation board equipped with a Virtex UltraScale xcvu095 FPGA and the power consumption of the entire board was measured by a watt checker plugged in to the AC power line. On the other hand, the power consumption for the GPU implementation was estimated from the thermal design power (TDP) of the devices.

Although the performance has not been reported in the literature, the latest GPUs (such as RTX3080) might outperform the FPGA implementation. However, the latest GPU consumes as much as 320 W. On the other hand, the FPGA implementation on the VCU108 evaluation board was about 20 W. One of the advantages of the FPGA approach is a high degree of energy efficiency with a relatively slow clock frequency.

### 4.3 Accuracy evaluation

Since the proposed approach is an approximate algorithm, accuracy of results is an important factor. When two adjacent scan vectors \( S_0 \) and \( S_1 \) detect two convex hull vertices \( V_i \) and \( V_{i+1} \), let \( C_i \) be a cross point of the two perpendicular line as shown in Fig 12. If other convex hull vertices exist inside the triangle \( V_iV_{i+1}C_i \), they will be overlooked since the triangle is a “shadow” of the projection. Qualitatively, an increase in the number of scan vectors \( s \) will increase the accuracy by reducing the angle between the two adjacent scan vectors and the shadow area. However, the probability of overlook largely depends on the shape of the convex hull and thus general formal modeling is not straightforward. Therefore, we experimentally performed the accuracy evaluation.

Fig. 13, 14, and 15 show the evaluation results of approximation metrics: \( r \), \( \mu \), and \( \eta \), respectively. Only four approximate convex hulls achieved \( r \) of 100\%. Especially, \( r \) values for the rbox group were relatively low, ranging 36.5\% to 84\%. However, the maximum \( \mu \) value was 3.809e-04. This means that the maximum difference between the polygons is 0.038% of the diameter, which is acceptable in most practical applications. Furthermore, the value of \( \eta \), the maximum value of the relative error in the area, was only 3.770e-04. These results suggest that the proposed algorithm can be used to find appropriate convex polygons to roughly grab abstract object shapes in applications such as collision detection. The largest error was observed when \( s = 50 \) for all the point sets. The error decreases as \( s \) increases, and the smallest error was shown when \( s = 350 \) for most point sets.

In this paper, we discussed only for 2D cases. For three or larger dimensions, theoretically, the vertices of the convex

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\(^{1}\)Estimated value from the graph
Table 5

<table>
<thead>
<tr>
<th></th>
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<td>2M</td>
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<td>20</td>
<td>10.6</td>
<td>53.1</td>
<td>0.21</td>
</tr>
</tbody>
</table>

5. Conclusion

In this paper, we proposed an approximate convex hull algorithm, which is oriented for hardware implementation in a sense that input points can be processed in a pipelined manner without storing all the points in memory. Then, the proposed algorithm was implemented on FPGA without external memory and the performance and accuracy were evaluated. Unlike the related work such as [11], our approach does not need to sort the input point set in advance. In addition, by changing the design parameter $s$, which is a discrete resolution of a scan vector, different trade-off points among hardware resources, performance, and approximation quality can be selected depending on application requirements. In the case of $s = 50$, up to 30 times performance was achieved, compared to the software library Qhull. The maximum approximation error metrics $\mu$ and $\eta$ were only 3.809e-04 and 3.770e-04, respectively. The evaluation results suggest our approach is effective in many practical real-time application domains. Expansion of the proposed method to 3D convex hull problems is one of our interesting future work.

References


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