
FOREWORD

Special Section on Reconfigurable Systems

The term *Reconfigurable System* comes from changing its own hardware configuration according to the target application for optimal processing. By this feature, Reconfigurable Systems can provide the characteristics of both high performance and high flexibility. However, framework for Reconfigurable System is not just an extension of traditional software and hardware technologies, and rather it is a superset including it. Run-Time and Dynamic Reconfiguration are characterized by the ability of underlying hardware architectures or devices to rapidly alter (on the fly) the functionalities of its components and the interconnection between them to suit the problem. It can become a powerful computing paradigm. For such Reconfigurable Systems to become a more practical technology in the industry, it is important to advance researches and developments on application, system software, computer architecture, and device technology.

Considering these situations, we planned a special section in order to survey the recent technical trend and forecast the future direction of Reconfigurable Systems. In response to the call for papers for this special section, 29 regular papers and three letters were submitted. Through the same review and editorial process as the regular section, 9 papers and one letter were accepted for publication. The selected papers will give readers the latest results in the research fields of reconfigurable systems, reconfigurable devices, applications and design tools for them.

The Special Section Editorial Committee Members listed below wish to thank all of those who submitted papers for consideration, as well as the reviewers for their thoughtful comments and suggestions. As the Guest Editor, I would like to express my sincere thanks to the Editorial Committee Members for their efforts to maintain the quality of the selected papers high. Also I would like to express my deep thanks to all the authors who submitted papers to this section.

The Special Section Editorial Committee Members:

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Toshinori Sueyoshi, Guest Editor

Toshinori Sueyoshi (*Member*) received the B.E. and M.E. degrees in Computer Science and Communication Engineering from Kyushu University in 1976 and 1978 respectively. From 1978 to 1987, he was a research associate at Kyushu University, where he received D.E. degree in Computer Science and Communication Engineering in 1986. From 1987 to 1989, he was an associate professor in the Interdisciplinary Graduate School of Engineering Sciences at Kyushu University. From 1989 to 1997, he was an associate professor in the Department of Artificial Intelligence at Kyushu Institute of Technology. From 1997 to 2006, he was a professor in the Department of Computer Science at Kumamoto University. Since 2006 he has been a professor of Computer Science and Electrical Engineering in the Graduate School of Science and Technology at Kumamoto University. He is also a guest professor at Kyushu University. His primary research interests include reconfigurable systems, computer architecture, parallel processing, system software, communication network, VLSI device and design. He is a member of IEEE, IEEJ and IPSJ. From 2005 to 2007, he served as Chair of the Technical Committee on Reconfigurable Systems of the IEICE Information and Systems Society. Currently he also serves as Chief Director of the Non-Profit Organization (NPO) named "FPGA consortium", Chair of the IEEE Computer Society Fukuoka Chapter, and Chair of the Technical Committee on Computer Systems of the IEICE Information and Systems Society.

