

Technology of FinFET for High RF and Analog/Mixed-Signal Performance Circuits

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SUMMARY In this paper, we discuss the process, layout and device technologies of FinFET to obtain high RF and analog/mixed-signal performance circuits. The fin patterning due to Side-wall transfer (SWT) technique is useful to not only fabricate narrow fin line but also suppress the fin width variation comparing with ArF and EB lithography. The H₂ annealing after Si etching is useful for not only to improve the mobility of electron and hole but also to reduce flicker noise of FinFET. The noise decreases as the scaling of fin width and that of FinFET with below 50 nm fin width is satisfied with the requirement from 25 nm technology node in ITRS roadmap 2013. This lower noise is attributed to the decrease of electric field from the channel to the gate electrode. Additionally, the optimum layout of FinFET is discussed for RF performance. In order to obtain higher f_T and f_{max} , it is necessary to have the optimized finger length and reduced capacitances between the gate and Si substrate and between gate and source, drain contact region. According to our estimation, the f_T of FinFET with the optimized layout should be lower than that of planar MOSFET when the gate length is longer than 10 nm due to larger gate capacitance. In conclusion, FinFET is suitable for high performance digital and analog/mixed-signal circuits. On the other hand, planar MOSFET is better rather than FinFET for RF circuits.

key words: FinFET, analog, RF, flicker noise, f_T , f_{max}

1. Introduction

Both higher on current and lower off current are required for high speed and low power consumption digital circuits. The scaled planar MOSFET has led to the higher speed application; however, the poor cut-off characteristics have been a serious problem with the scaling of the gate length. Recently, un-doped double gate MOSFETs, such as FinFET are promising candidates for scaling CMOS into the sub-22 nm node and below because of its good cut-off characteristics and better scalability due to double gate mode operation. As the scaling of CMOS has been progressed, RF CMOS has been popular because of higher f_T and f_{max} with below 0.25 μm gate length. RF designers are interested in f_T , f_{max} of FinFET for future application; however, reported those values of FinFET are lower than planar MOSFET [1], [2]. In this paper, we discuss process, layout and device technologies of FinFET to obtain higher RF performance. Additionally, structural merits of FinFET relative to flicker noise are also discussed.

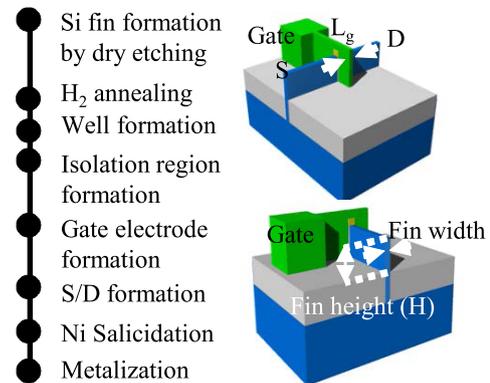


Fig. 1 Process flow to fabricate Fin FET. H₂ annealing after Si dry etching is carried out to reduce trap density [10].

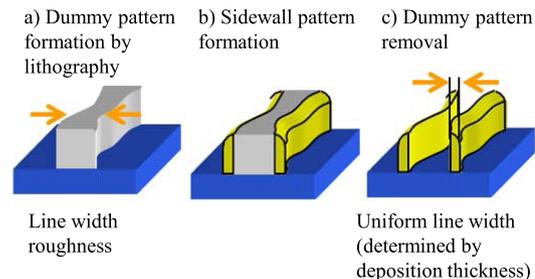


Fig. 2 Process steps of sidewall-transfer technique for the fabrication of narrow gate width FinFET.

2. Sample Fabrication

2.1 Process Flow

Planar MOSFET has a gate electrode on Si substrate, while gate electrodes surround Si substrate in fin FET to suppress the short channel effect as the gate length is below 20 nm. Figure 1 shows schematic view of our FinFET structure and process flow [3]–[10]. The Si surface of the channel was (110) because the FinFET was fabricated on standard (100) Si substrate. Narrow fins below 20 nm width were formed by side-wall transfer (SWT) technique [3], [4]. After RIE (Reactive Ion Etching) of Si, H₂ annealing was carried out to improve the gate oxide quality and reduce trap density of the Si surface, the gate stack was formed by SiON gate dielectrics and poly-Si.

SWT technique and its process are shown in Fig. 2. After SiO₂ film deposition, the patterning was carried out

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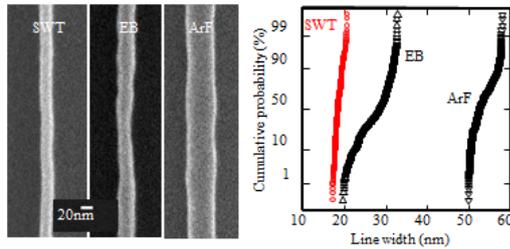


Fig. 3 Comparison of fin line width and variation in SWT, EB and ArF lithography and cumulative probability of line width after RIE are shown. Each target of line width was set to the minimum size available in each lithography technology. SWT is successful in below 20 nm fin line with the small variation [10].

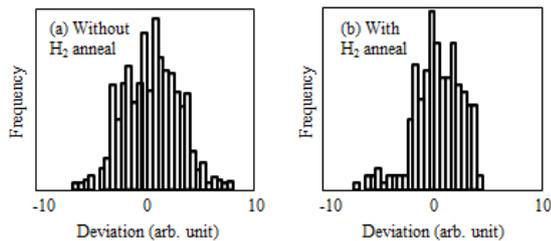


Fig. 4 Surface roughness with and without H₂ annealing. The roughness was improved by the annealing after dry etching.

by ArF lithography, which is used as dummy line. After SiN film was deposited on the patterned SiO₂ film, sidewall spacer was fabricated by dry etching of SiN film and this region was used as hard mask for fin pattern during Si dry etching. The line to be formed by the sidewall spacer is narrower than the original dummy line pattern and has good LWR (Line Width Roughness) uniformity even if the uniformity of the dummy SiO₂ line width was poor because the line width is determined by the deposition thickness of SiN film not by lithography. The dummy SiO₂ line is removed by wet treatment.

Figure 3 shows top-view SEM images and cumulative probability results of fine line patterns fabricated by SWT, EB lithography and ArF lithography, respectively. The width is narrower and the uniformity in SWT technique is better than those in EB and ArF lithography as shown in cumulative probability results of line width. The better uniformity of fin line width is effective for suppression of larger drain current variation.

2.2 Effect of H₂ Annealing

The performance of FinFET is very sensitive to the surface quality of the etched surface of the Si fin, which serves as the channel layer. It is therefore important to improve the surface quality of the Si fin. Figure 4 shows surface roughness of Si surface with and without H₂ annealing after Si etching. The roughness was improved thanks to the annealing because atomically flat or regularly arranged steps on the surface have been realized due to the migration of Si atoms on the surface during H₂ annealing [9], [10]. In order to evaluate the quality of Si surface after H₂ annealing,

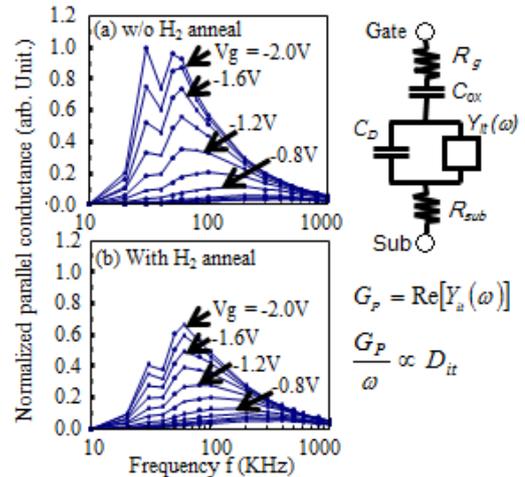


Fig. 5 Interface trap density between Fin surface and gate oxide estimated by parallel-conductance method. The density becomes lower due to hydrogen anneal.

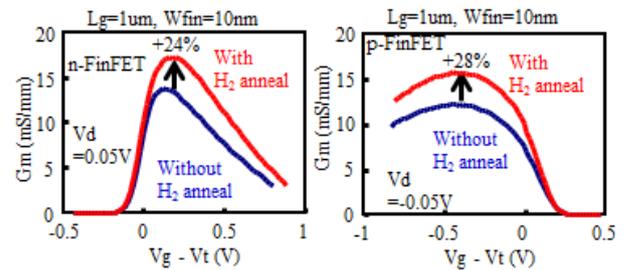


Fig. 6 The transconductance comparison for n- and p-FinFET with and without hydrogen anneal. These conductance are improved because of lower interface trap density.

the parallel conductance of MOS capacitor of FinFET was measured. The equivalent circuit of MOS structure of FinFET is shown in Fig. 5. R_g , C_{ox} and C_d are gate resistance, gate insulator capacitance and depletion capacitance under gate insulator, respectively. Y_{it} is the admittance of depletion region. The value of real part of Y_{it} divided by measurement frequency (Y_{it}/ω) is proportional to interface trap density between gate insulator and Si substrate. The divided Y_{it} of FinFET with H₂ annealing is about 30% lower than without H₂ annealing as shown in Fig. 5(a) and (b). These results show not only roughness of Si surface but also the quality of Si surface after Si etching is improved due to the H₂ annealing process.

Figure 6 shows gate voltage dependence of transconductance of both FinFET in linear region for n-FinFET and p-FinFET. The transconductance of FinFET with H₂ annealing process are larger than that without the annealing and the peak values of n-FinFET and p-FinFET become 24 and 28% larger, respectively. These should be attributed to the improvement of the mobility of electron and hole of FinFET due to improvement of Si surface quality.

3. Analog Performance

Lower flicker noise is essential requirement for analog/

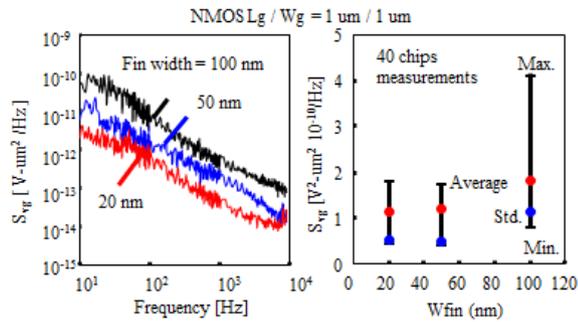


Fig. 7 Fin width dependence of n-FinFET flicker noise and the variation of the noise. The noise and the variation become lower as the scaling of the width [12].

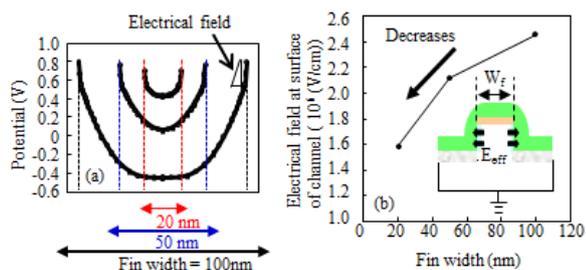


Fig. 8 Dependence potential profile on fin width. The slope of the potential in the channel becomes lower as shown in this figure. That means vertical electrical field from channel to gate electrode becomes relaxed. This relaxation causes the decrease of trap rate and flicker noise [12].

mixed-signal circuits such as voltage controlled oscillator (VCO), analog-to-digital converter (ADC) and so on. It is therefore important to reduce the noise of FinFET for the application to those circuits. The noise characteristics of FinFET have been reported in some technical journals and conferences [12]–[15]. We focus on fin width dependence of the noise and analyze the dependence by using our simulator for the first time. The H_2 annealing was carried out to the measured samples because the noise is sensitive to the interface trap density between the gate insulator and Si substrate.

Figure 7 shows fin width dependence of n-FinFET input-referred flicker noise (S_{vg}) in saturation region. These noises are normalized by multiplying by gate area (L_g times W_g). The range of fin width was from 100 nm to 10 nm, and the gate length and total gate width were $1 \mu\text{m}$ and $1 \mu\text{m}$, respectively. In this figure, average, minimum and maximum values in 40 devices are shown. It is clear that not only the noise itself but also the variation decreases as the fin width becomes below 50 nm. According to the results of substrate bias dependence of V_{th} , the FinFET with 100 nm fin width is in partial depletion mode, while those with below 50 nm fin width are in fully depletion mode like an ultra thin body FD silicon on insulator devices (UTB FD SOI devices).

To analyze the origin the noise reduction below 50 nm fin width, electric field from channel to gate electrode, which works as force to trap into gate insulator, is calculated by our device simulator as shown in Fig 8(a). The potential of center of fin abruptly approaches the surface potential

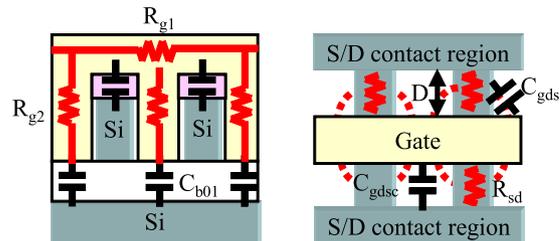


Fig. 9 Parasitic resistance and capacitance for FinFET. Resistance of vertical gate electrode (R_{g2}), S/D (R_{sd}), capacitance of gate-Si sub. (C_{b01}), gate-S/D (C_{gds}) and gate-S/D con. Region (C_{gdsc}) have large impact for RF performance [22].

with scaling fin width. As a result, the slope of the potential at Si surface decreases. This electric field works as the force to be trapped for electrons in the channel of FinFET. Figure 8(b) shows the fin width dependence of the electrical field at surface of channel calculated based on Fig. 8(a). The simulation results show the field is relaxed along with fin width narrowing. Some papers reported flicker noise of MOSFET on UTB FD SOI devices with fully depletion mode and larger flicker noise reduction was observed [16]. We think the lower flicker noise with below 50 nm fin width is caused by the lower the electrical field. The minimum noise level of FinFET with below 50 nm fin width is satisfied with the requirement for 25 nm technology node in ITRS roadmap 2013 [17]. These results show FinFET is useful and applicable device for analog/mixed-signal circuits.

4. RF Performance

Some papers reported how to estimate parasitic resistance and capacitance [18]–[22] in scaled MOSFETs. We calculated the transconductance and the gate capacitance based on these paper and estimated f_T and f_{max} of FinFET. Figure 9 shows schematic view of our multi finger FinFET structure. To calculate f_T and f_{max} , the parasitic capacitance and resistance are estimated with considering the following parameters; gate length, fin width, gate width, finger length, fin pitch, fin height, STI depth, distance between gate electrode and source & drain contact region and the gate material. For example, when the impact of the gate resistance is calculated, not only top gate but also buried gate electrode between fins should be considered. The parasitic resistance of source and drain (R_{sd}) is calculated in considered of fin width and sheet resistance of Ni silicide. Gate capacitance to Si substrate between fins (C_{b01}) and coupling with source, drain contact region (C_{gsdc}) are also considered.

Figure 10 shows the simulation results of fin pitch dependence of f_T and f_{max} when gate length is 30 nm. The main parameter is distance between gate electrode and source, drain contact region (D). Both f_T and f_{max} increase as the fin pitch size decreases because of smaller C_{b01} . The f_T value, however, decreases significantly due to larger gate capacitance (C_{gsdc}) when the source, drain contact region closes to the gate electrode. When the material of buried gate electrode is doped poly Si, f_{max} degrades at small fin

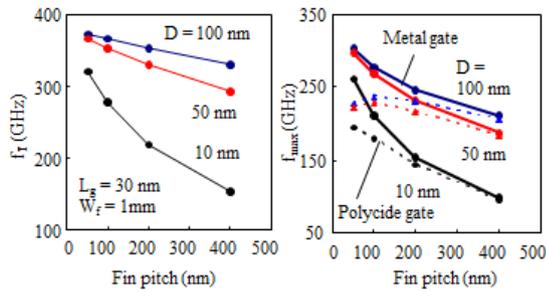


Fig. 10 Fin pitch dependence of f_T and f_{max} . Parameter D is distance between gate and source, drain contact region [22].

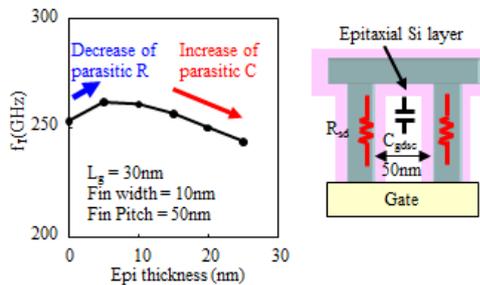


Fig. 11 Dependence of f_T on epitaxial Si thickness grown on Source and drain to reduce parasitic resistance [22].

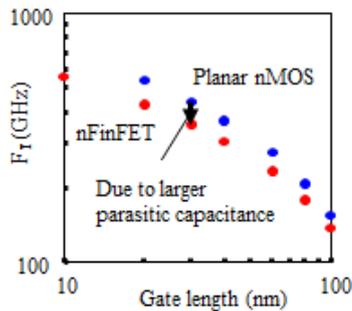


Fig. 12 f_T of nFinFET with the optimum layout design for RF performance. That is lower than planar nMOS below 20 nm gate length due to larger parasitic capacitance [22].

pitch due to increase of gate electrode resistance (R_{g2}). In our estimation, the most important device parameter is the finger length as well as planar MOSFET. Next, the distance between the gate and the source & drain contact region has higher impact to realize high f_T and f_{max} than the fin pitch and the fin height.

When epitaxial Si growth on source and drain is applied to reduce source and drain resistance, this unique S/D structure should be taken into consideration to evaluate the RF performance. Figure 11 shows the epitaxial Si thickness dependence of f_T when fin pitch is 50 nm. As epitaxial thickness increases, the f_T increases because the transconductance increases by decrease of parasitic resistance of source and drain, however, further increase of the epitaxial Si thickness beyond 10 nm causes the decreases of f_T because of the increase of parasitic capacitance between the gate and source, drain contact region (C_{gsdc}).

Figure 12 shows f_T of nFinFET with the optimum lay-

out design for RF performance. The estimated f_T values of planar nMOSFET are also plotted as reference. Those of FinFET are lower than planar nMOSFET beyond 10 nm gate length due to larger parasitic capacitance. These results show FinFET with longer gate length has the disadvantage for RF performance due to larger gate capacitance comparing with planar MOSFET [23].

Conclusion

Fin patterning due to Side-wall transfer (SWT) technique is useful to not only fabricate narrow fin line but also suppress fin width variation. The H_2 annealing after Si etching is useful for not only to improve the mobility of electron and hole but also to reduce flicker noise of FinFET. The noise in FinFET with fully depletion mode decreases which are similar to UTSOI devices. However, FinFET has the disadvantage for RF performance due to larger gate capacitance comparing with planar MOSFET.

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