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## FOREWORD

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### Special Section on Analog Circuits and Related SoC Integration Technologies

Analog circuits and related SoC integration are key technologies that enable the analog world we live in to interact with the digital world of computing. We expect that these technologies will progress steadily along with digital circuit technology. Despite the fact that analog design becomes more difficult as the process is scaled down to the deep submicron range, the performances of analog and RF CMOS integrated circuits have been continually improving. Researchers in this field have routinely proposed innovative ideas to overcome the difficulties encountered in analog design in deep submicron CMOS and to effectively exploit the advantages of finer transistors. The creativity of these researchers is the driving factor behind the progress made in analog designs.

I believe that the readers will find a variety of eye-opening ideas in this special section, which contains 20 papers selected from among 46 submissions by a rigorous review process. The selected papers include topics on elemental, although practical, analog and RF circuit blocks; wireless and wireline communication systems; mixed-signal circuit systems; and emerging applications.

In addition, this special section includes two invited papers. The first one, written by Boris Murmann — the well-known propounder of “digitally assisted analog circuits” — reviews the recent low-power ADC trend and provides in-depth insights. This paper reveals the previously not clear reasons behind the continuous ADC improvements. The second paper, written by Rui Ito and Tetsuro Itakura, focuses on the phase-compensation techniques of operational amplifiers and discusses these techniques from the view point of power efficiency. This paper would be quite beneficial for all analog engineers.

On behalf of the editorial committee, I would like to express my sincere appreciation to all those who submitted manuscripts for this special section and to all the reviewers. Lastly, I would like to thank all the editorial committee members, as listed below, for their enthusiastic support of the editorial work.

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#### Kunihiko Iizuka, Guest Editor-in-Chief

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**Kunihiko Iizuka** (*Member*) received B.S. and M.S. degrees in mathematics from Osaka University, Osaka, Japan, in 1979 and 1981, respectively. In 1984, he joined Sharp Corporation, Japan, where he was involved in the research of computer simulation systems. From 1991 to 1993, he was at the Center for Adaptive Systems, Boston University, Boston, MA, as a visiting researcher, working on neural network systems. Since 1993, he has been working on research and development of analog and mixed signal LSI circuits for high precision ADCs, vision systems, and wireless systems in Sharp. He was enrolled in postgraduate course of electronic engineering at Tokyo Institute of Technology from 2006 to 2009 and received the Ph.D. degree from the university in 2009 on the subject of RF and analog integrated circuits for television broadcast receivers. He is currently a chief technical research fellow of the company and the vice chair of IEEE SSCS Kansai Chapter.

