INVITED PAPER *Special Section on Cognitive Radio and Spectrum Sharing Technology*

Reconfigurable RF CMOS Circuit for Cognitive Radio

Kazuya MASU[†a)] ***and*** **Kenichi OKADA**[†b)], ***Members***

SUMMARY Cognitive radio and/or SDR (Software Defined Radio) inherently requires multi-band and multi standard wireless circuit. The circuit is implemented based on Si CMOS technology. In this article, the recent progress of Si RF CMOS is described and the reconfigurable RF CMOS circuit which was proposed by the authors is introduced. At the present and in the future, several kind of Si CMOS technology can be used for RF CMOS circuit implementation. The realistic RF CMOS circuit implementation toward cognitive and/or SDR is discussed.

key words: *CMOS, reconfigurable RF circuit, cognitive radio*

1. Introduction

Many kinds of wireless communication standards have become commercially available and currently in use, e.g., WLAN, Bluetooth, GPS, DTV, and RFID. Multi-mode mobile phone has become popular; the 3-band cellar phone is available at present time and 6-band cellar phone is expected to be realistic with in several years. In the concept of "Cognitive Radio," wireless terminals communicate using the frequency band and/or the standard that are not being used [1], [2]. Although there remain the license issues, the cognitive radio is expected to enhance the frequency usage efficiency. The cognitive radio inherently requires the multi-band/multi-mode wireless circuits. The concept Software Defined Radio (SDR) [2] presents that the RF/baseband circuit should operates depending on the software or control unit. Ultimately one circuit module can modulate and/or demodulate the various kind wireless standards.

Recent progress of Si CMOS LSI performance can enables the implementation of GHz range RF circuit, so that the commercial wireless equipment are implemented using Si CMOS. Reconfigurable RF CMOS circuit is one hardware solution for SDR and/or cognitive radio.

This paper describes (1) the recent progress of Si CMOS technology featuring the RF characteristics, (2) reconfigurable RF circuit and some circuit blocks. Finally, realistic RF CMOS implementation toward SDR and/or cognitive radio is discussed.

2. Si RF CMOS Circuit

Si CMOS has been miniaturized and exhibited the performance improvement based scaling law. Impact of miniaturization is not only performance improvement but also chip area reduction, resulting in cost reduction.

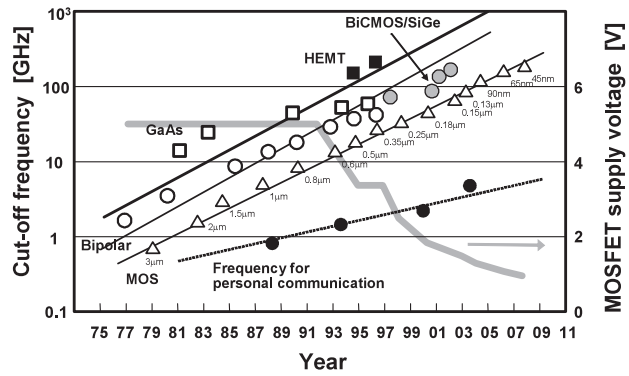


Fig. 1 Cut off frequencies of various kind devices and frequency for personal communication. The values attached to MOS data points are technology node of MOSFET, which is almost the same as 1st metal pitch. MOSFET supply voltage is also plotted.

Figure 1 shows cut-off frequencies of several devices. Present and future CMOS performance is summarized in ITRS publication [3]. The frequency band for cellular phone is 800 MHz in 1980's, and recently the frequency bands have expanded to 2.4/5 GHz. In 1980's the cut off frequency (f_t) of Si CMOS is a few GHz and RF CMOS application has started. In the digital circuit application, miniaturization of CMOS has brought the drastic MPU performance improvement. The cut-off frequency has also increased and recent sub-100 nm MOSFET has over 100 GHz cut-off frequency. The cut-off frequency is the frequency at which the current gain becomes unity. The maximum frequency of oscillation (f_{max}) at which the unilateral power gain unity has also improved. The recent Si MOSFET has sufficient performance for GHz range application from the view point of f_t and f_{max} and recently CMOS circuit for 60–90 GHz millimeter application is progressing. As gate length is reduced, the supply voltage becomes lower as shown in Fig. 1. The supply voltage V_{dd} is 1.8 V for 180 nm, 1.2 V for 90 nm CMOS. In the state-of-art 65 nm/45 nm CMOS, the voltage is becomes less than 1 volt. As described later, the reduction of supply voltage brings the design difficulties.

In the digital application, the threshold voltage and saturation current of MOSFET are the most important parameters. In the RF CMOS circuit, more accurate MOSFET model is required; current-voltage characteristics en-

Manuscript received October 23, 2007.

[†]The authors are with Integrated Research Institute, Tokyo Institute of Technology, Yokohama-shi, 226-8503 Japan.
a) E-mail: masu@pi.titech.ac.jp
b) E-mail: okada@pi.titech.ac.jp

DOI: 10.1093/ietcom/e91–b.1.10

Copyright © 2008 The Institute of Electronics, Information and Communication Engineers

tire range and noise model, etc. In RF CMOS circuit, high-Q passives such as inductor and capacitor play important role. Requirement for capacitor is small area; the so-called MIM capacitor which is fabricated using thin high-k film is prepared. In GHz application, nH-order inductors are used, and can be implemented as on-chip spiral inductor. However, the issues are low-Q value due to metal wire resistance itself and eddy current loss of resistive Si substrate. If one uses the standard CMOS process where the metal thickness is around 1 μm, the Q-value is around 3-5. Using the around 3 μm-thick metal at the top layer of multilevel interconnect structure, the Q-value can be improved to be over 10. Introduction of the MIM capacitor and thick metal inductor is called as *RF option*. It is noted that the use of *RF option* brings the cost increase. Here, it is pointed out that inductor requires large area. The impact of inductor area is discussed later.

The conventional super heterodyne architecture requires IF filter, which cannot be implemented on chip. The direct conversion architecture [4] has been widely utilized toward one chip implementation. We have proposed Reconfigurable RF CMOS circuit which consist of digital and analog/RF circuit blocks [5], [6] as shown in Fig. 2. The transceiver is fundamentally based on the direct conversion architecture. The proposed design concept has two features: (1) the multi-band and multi-mode RF circuit, and (2) the dynamic self compensation. Each circuit module in RF front-end is tunable and/or wide band characteristics. The proposed architecture aims to achieve these wireless communication functions by only one reconfigurable RF circuit, which can be used for SDR and/or cognitive radio application. On the other hand, the dynamic self compensation provides the reduction of design cost, the robustness against the process variations, simulation errors, etc. In the scaled MOSFETs, fluctuation of device and passive characteristics is inevitable, so that the digital enhanced self compensation technique become more important.

So far, we have developed wide band VCOs [7]–[10], tunable LNA using variable inductor [11], wideband LAN [12]. In this paper, wide tuning range VCO is described.

Figure 3(a) schematizes a LC-VCO using the on-chip variable inductor and varactor and three switched capacitors. Each switched capacitor is composed of N-MOS gate capacitors and N-MOS switches. Capacitances of the switched capacitors are 100 fF ($C1$), 200 fF ($C2$) and 400 fF ($C3$). The principle of the variable inductor is as follows; (1) the variable inductor consists of the conventional on-chip spiral inductor, and metal plate whose size is larger than the spiral inductor and which is place above the inductor, (2) the change of the distance between the inductor and metal plate gives the inductance change. The metal plate is assumed to be moved by MEMS actuator. Figure 3(b) shows a chip micrograph of fabricated VCO. The VCO core area is $400 \times 600\,\mu$m. Table 1 summarizes the VCO performance. Recently, we have proposed and implemented the wide band LC-VCO with frequency expand circuit [9], [10], where the variable inductor is not utilized. As listed in Table 1, the

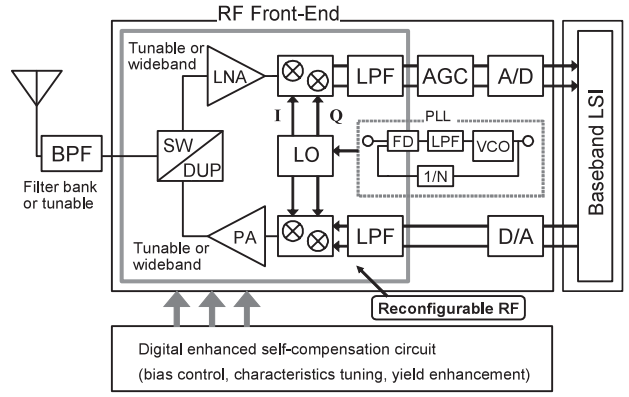
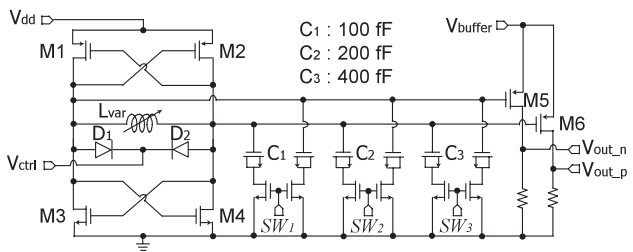
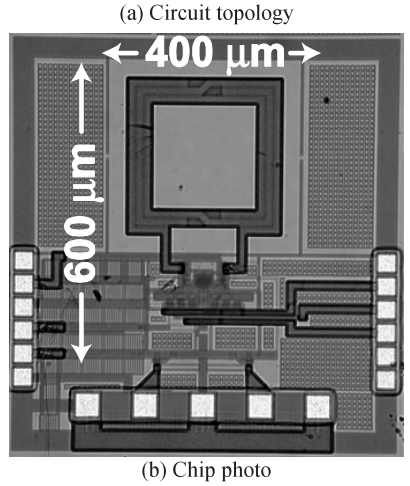


Fig. 2 Direct conversion type redonfigurable RF CMOS circuit.



(a) Circuit topology



(b) Chip photo

Fig. 3 Wide band voltage controlled oscillator using variable inductor [8].

tuning range is from 0.5 GHz to 6.5 GHz; this tuning range is enough for application to DTV at 470–770 MHz, mobile phones, and WLAN at 2.4/5 GHz. $\mathrm{FOM_T}$ is known to be a parameter for evaluating VCOs by taking into account the phase noise as well as tuning range [13]. The $\mathrm{FOM_T}$ of VCOs are below −205 dB/Hz, which is the highest value among the reported ones.

As seen in Fig. 3(b), the inductor area is $400\,\mu$m$\times$ $400\,\mu$m, on the other hand, the MOSFET area is much less than the inductor area. The inductor area is determined by the value of inductor, i.e., nH-order inductor requires hundred μm□ area. Generally, inductor area of one-chip-chip Bruetooth or WLAN LSI is know to be 20–30% using 180–130 nm CMOS process. Emphasis is the required inductor

Table 1 LC-VCO performance.

Technology	180nm standard CMOS using variable inductor [8]	180nm CMOS with RF option Frequency expand technique is utilized. [10]
Supply voltage (V_{DD})	1.8V	1.8 V
VCO core current	9.8 –13 mA	4.6 – 14.4 mA
Power consumption	18 – 24mW	8.4 – 25.9 mW
Center frequency	2.02 GHz	3.49 GHz
Tuning range	1.28 -2.75 GHz (72%)	0.49 – 6.50 GHz FTR = 172%
Phase noise at 1MHz offset	135 dBc/Hz @2.02 GHz	-180 dBc/Hz @2.41 GHz
FoM_T	-206 dBc/Hz @2.02 GHz	-205 dBc/Hz @2.41 GHz

$$FOM_T = L\{f_{\text{offset}}\} - 20\log\left(\frac{f_{\text{offset}}}{f_{\text{offset}}} \cdot \frac{FTR}{10}\right) + 10\log\left(\frac{P_{\text{DC}}}{1mW}\right)$$

where $L\{f_{\text{offset}}\}$ is phase noise at f_{offset}, f_{offset} is certain frequency offset, f_o is center frequency, P_{DC} is the power consumption, and FTR is tuning range of oscillation frequency.

area cannot be reduced even using the scaled MOSFET technology.

3. Solutions for Reconfigurable RF CMOS

Present multi-band transceiver involves plural Tx/Rx circuit. So called one chip implementation seems to be suitable for reconfigurable RF CMOS, which will be utilized in cognitive radio and/or SDR. In this paper, it is pointed out that the development of RF CMOS circuit should be performed, depending on the process technology and manufacturing cost.

The advantage of the use of scaled CMOS is not induced without cost reduction. The cost reduction is originated from the area reduction using the scaled CMOS process. As pointed out in the previous section, at the GHz frequency range, the required inductor value is not scaled; this means that, if the inductor is utilized, cost reduction cannot be expected in the scaled CMOS process.

Figure 4 presents the development of RF front end. The improvement of RF circuit performance is directrly related to the Q-value of the inductor, so that the RF circuit with cost effective high-Q passives such as the used of WLP(Wafer Level Packaging)-inductor [14] is promising. For area saving for cost reduction, development of inductor less circuit is required; *ex*. Resistive-feedback LNA [15]. DRP (Digital Radio Processing) has been proposed and developed [16], [17]. These kind of digital processing and digital enhanced architecture become to replace the conventional analog part. The issues is area penalty and power penalty should not be induced.

From the viewpoint of transceiver and system implementation, it is pointed out there are various approach besides one chip solution where RF, baseband, and filters are all implemented. From the view point of foundry, circuit designer can use various kind of process line; wafer size of 6,' 8,' and 12,' process technology from 0.25 μm to the state-of-art 65 nm/45 nm, and "with" or "without" RF option. Using the mature process technology, the design and fabrication cost is low, so that SiP (System in Package), CoC (Chip on Chip), Chip Stacking, 3D integration technique is promising.

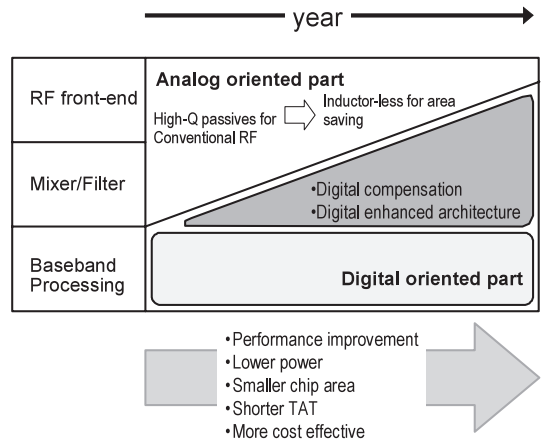


Fig. 4 RF CMOS circuit trend.

Since the fully one solution is always the best way, appropriate approach should be used, depending on the required TAT, cost and performance,

4. Conclusion

In this paper, we discussed reconfigurable RF CMOS technology for cognitive radio and/or SDR. It is pointed out there are various approaches for reconfigurable RF CMOS circuits.

Acknowledgments

This work was partially supported by JSPS.KAKENHI, MEXT.KAKENHI STARC, SCOPE, NEDO, Fujiraku, intel, and VDEC in collaboration with Cadence Design Systems, Inc. and Synopsys, Inc. The authors thank graduate students of Masu research group for their contribution to this work.

References

[1] J. Mitola, "Cognitive radio for flexible mobile multimedia communications," Proc. Mobile Multimedia Commoiun. (MoMuC'99), pp.3–10, Nov. 1999.
[2] D. Murotake, "Markets committee status," SDR document number, SDRF-06-1-0008-V0.00, June 2006, (downloadable from http://sdrforum.org/)
[3] International Technology Roadmap for Semiconductors, 2005, see http://public.itrs.net/

[4] A.A. Abidi, "Direct-conversion radio transceivers for digital communications," IEEE J. Solid-State Circuits, vol.30, no.12, pp.1399–1410, 1995.

[5] K. Okada, Y. Yoshihara, H. Sugawara, and K. Masu, "A dynamic reconfigurable RF circuit architecture," IEEE/ACM Asia South Pacific Design Automation Conference, pp.683–686, Jan. 2005.

[6] K. Okada, Y. Yoshihara, H. Sugawara, and K. Masu, "Design of reconfigurable RF CMOS wireless circuit," IEICE Trans. Electron. (Japanese Edition), vol.J89-C, no.7, pp.499–507, July 2006.

[7] Y. Yoshihara, H. Sugawara, H. Ito, K. Okada, and K. Masu, "Wide tuning range LC-VCO using variable inductor for reconfigurable RF circuit," IEICE Trans. Fundamentals, vol.E88-A, no.2, pp.507–512, Feb. 2005.

[8] Y. Ito, Y. Yoshihara, H. Sugawara, K. Okada, and K. Masu, "A 1.3–2.8 GHz wide range CMOS LC-VCO using variable inductor," IEEE Asian Solid-State Circuits Conference, pp.265–268, Nov. 2005.

[9] Y. Ito, H. Sugawara, K. Okada, and K. Masu, "A 0.98 to 6.6 GHz tunable wideband VCO in a 180 nm CMOS technology for reconfigurable radio transceiver," IEEE Asian Solid-State Circuits Conference (A-SSCC), pp.359–362, Hangzhou, China, Nov. 2006.

[10] Y. Kobayashi, K. Ohashi, Y. Ito, H. Ito, K. Okada, and K. Masu, "A 0.49–6.50 GHz wideband LC-VCO with High-IRR in a 180 nm CMOS technology," International Conf. on Solid State Devices and Materials (SSDM), pp.268–269, Tukuba, Sept. 2007.

[11] H. Sugawara, Y. Yoshihara, K. Okada, and K. Masu, "Reconfigurable CMOS LNA for software defined radio using variable inductor," IEEE MTT-S European Microwave Conference, pp.1947–1950, Oct. 2005.

[12] T. Ito, D. Kawazoe, K. Okada, and K. Masu, "A DC-7 GHz small-area distributed amplifier using 5-port inductors in a 180 nm Si CMOS technology," IEEE Asian Solid-State Circuits Conference (A-SSCC), pp.359–362, Hangzhou, China, Nov. 2006.

[13] Y.T. Wang and A.A. Abidi, "CMOS active filter design at very high frequencies," IEEE J. Solid-State Circuits, vol.25, no.6, pp.1562–1574, Dec. 1990.

[14] H. Hatakeyama, K. Okada, K. Ohashi, Y. Ito, N. Ozawa, M. Sato, T. Aizawa, T. Ito, R. Yamauchi, and K. Masu, "Application to 5.8 GHz LC-type voltage controlled oscillator," Advanced Metallization Conference, pp.8–9, Albany, Oct. 2007

[15] J.-H.C. Zhan and S.S. Taylor, "A 5 GHz resistive-feedback CMOS LNA for low-cost multi-standard applications," IEEE Internarional Solid State Circuit Conference (SSCC), pp.200–201, 2006.

[16] R.B. Staszewski, K. Muhammad, D. Leipold, C.-M. Hung, Y.-C. Ho, J.L. Wallberg, C. Fernando, K. Maggio, R. Staszewski, T. Jung, J. Koh, S. John, I.Y. Deng, V. Sarda, O. Moreira-Tamayo, V. Mayega, R. Katz, O. Friedman, O.E. Eliezer, E. de Obaldia, and P.T. Balsara, "ALL-digital TX frequency synthesizer and discrete-time receiver for bluetooth radio in 130 nm CMOS," IEEE J. Solid-State Circuits, vol.39, no.12, pp.2278–2291, 2004.

[17] R.B. Staszewski, J. Wallberg, S. Rezeq, C.M. Hung, O. Eliezer, S. Vemulapalli, C. Fernando, K. Maggio, R. Staszewski, N. Barton, M.C. Lee, P. Cruise, M. Entezari, K. Muhammad, and D. Leipold, "ALL-digital PLL and GSM/EDGE transmitter in 90 nm CMOS," IEEE International Solid-State Circuits Conf., pp.316–317, 2005.

Kazuya Masu received the B.E., M.E. and Ph.D. degrees in Electronics Engineering from Tokyo Institute of Technology, Tokyo, Japan, in 1977, 1979 and 1982, respectively. He was with the Research Institute of Electrical Communication, Tohoku University, Sendai, Japan since 1982. In 2000, he moved to Precision and Intelligence Laboratory, Tokyo Institute of Technology, Yokohama, Japan and he is currently a professor in Integrated Research Institute, Tokyo Institute of Technology. He was a visiting Professor in Georgia Institute of Technology in 2002 and 2005. His current interests are signal integrity and GHz signal propagation in multilevel interconnect of Si ULSI, reconfigurable RF circuit technology, performance evaluation and prediction based on interconnect wire length distribution, and BEOL process technology. He received IEICE Electronics Society Award in 2005. He is a member of the IEEE, the Japan Society of Applied Physics (JSAP), the Institute of Electrical Engineers of Japan (IEEJ), Japan Institute of Electronics Packaging (JIEP), and the Electrochemical Society (ECS).

Kenichi Okada received the B.E., M.E. and Ph.D. degrees in Communications and Computer Engineering from Kyoto University, Kyoto, Japan, in 1998, 2000, and 2003, respectively. From 2000 to 2003, he was a Research Fellow of the Japan Society for the Promotion of Science. From 2003, he was with Precision and Intelligence Laboratory, Tokyo Institute of Technology, Yokohama, Japan and he is currently an associate Professor in Department of Physical Electronics, Tokyo Institute of Technology. His research interests include computer-aided-design for statistical analysis and RF circuit design. He is a member of IEEE, the Information Processing Society of Japan (IPSJ), and the Japan Society of Applied Physics (JSAP).