SUMMARY

We review the recent achievements in monolithic 3D-ICs and flexible electronics based on single-grain Si TFTs that are fabricated inside a single-grain with a low-temperature process. Based on pulsed-laser crystallization and amorphous-Si precursor film was converted into poly-Si having grains that are formed on predetermined positions. Using the method called Czochralski process and LPCVD a-Si precursor film, two layers of the Si TFT layers with the grains having a diameter of 6 µm were vertically stacked with a maximum process temperature of 550 °C. Mobility for electrons and holes were 600 cm²/Vs and 200 cm²/Vs, respectively. As a demonstration of monolithic 3D-ICs, the two SG-TFT layers were successively implemented into CMOS inverter. 3D 6T-SRAM and single-grain lateral PIN photo-diode with in-pixel amplifier. The Si Si TFTs were applied to flexible electronics. In this case, the a-Si precursor was prepared by doctor-blade coating of liquid-Si based on pure cyclotetrasilane (CPS) on a polyimide (PI) substrate with a low-manufacturing cost, it will give a great impact to the future era of internet-of-things. To realize such device, two drastic changes in the electronic device fabrication seem to be the solution, namely, three-dimensional integrated circuits (3D-ICs) and flexible electronics.

The 3D-ICs, in which active devices are vertically stacked upon each other separated by insulating layers, will break-through the problems of the conventional 2D-ICs [1], [2]. Since the 3D-ICs can realize a high integration density, a compact overall system, short and dense interconnects and increased functionality, this will facilitate More than Moore approach in IC industry. Among various 3D integration technologies, monolithic 3D integration [3], [4] allows transistor level integration and therefore provides the highest density of vertical interconnects between the stacked layers. Here the Si layer must be newly formed on ILD at each level of the IC and therefore the crystalline quality of the layer is very important aspect for successful implantation. In the past, monolithic integration has been demonstrated with solid phase crystallization (SPC). Because the poly-Si consists of many grains, dense random grain boundaries (GBs) between the grains deteriorates mobility in the on-state and also create a leakage path in the off-state. More recently 3D SRAM has been demonstrated with epitaxially grown Si from crystalline-Si substrate as seeds using laser crystallization [5]. The process requires, however, high temperature (> 600 °C) for the vertical epitaxial growth from the seeding substrate by solid-phase recrystallization and this will thermally deteriorate the underlying devices. Technical bottleneck so far in the monolithic 3D-ICs is therefore either the poor semiconductor layer quality or the high process temperature.

Flexible electronics will open novel applications in, not only displays, but also RF-ID tag and sensors because of the large area, freedom in the form-factor and low-cost manufacturing. Here printing process and low-temperature process which is compatible with plastic substrate are very important [6]. Organic [7] and metal oxide [8] semiconductors are able to meet these two requirements and therefore many research have been performed based on those materials. While the transistor performance has been improving over the last decade, carrier mobility and reliability of TFTs using those materials are far less than those using silicon. Transferring of CMOS-SOI chips by chemical etching [9] and amorphous Si (a-Si) transistors on plastics by laser release [10] have been reported. However the former has cost and technical issues since the limited size of the wafer and pick and place process, and in the latter, the electrical performance is low, although the laser release technique requires lesser cost. On the other hand, poly-Si TFTs can be fab-
ricated on a plastic substrate [11] because of the short diffusion length during the pulsed-laser crystallization process [12], [13]. The mobilities of the poly-Si TFTs are, however, still much lower than those of the crystalline-silicon devices, and the fabrication is still based on vacuum and non-printing process.

In this paper we propose monolithic 3D ICs and flexible electronics based on “single-grain” (SG) Si TFTs where transistors are fabricated inside a silicon grain with a low-temperature process. Location and crystallographic-orientation of the grain are accurately controlled by the method called μ-Czochralski process, which is based on pulsed-laser crystallization and hence does not thermally deteriorate the underlying device layers. Single-crystalline Si wafers are not needed and therefore the process can be applied to a low-temperature resistant substrate, such as a glass or a flexible plastic. After reviewing the μ-Czochralski process, fabrication process of stacking of two layers of single-grain Si TFTs will be explained. With two SG-TFT layers CMOS inverter, SRAM and lateral photodiodes with an in-pixel amplifier have been designed and monolithically stacked upon each other. For the flexible electronics application, printing process has been used for preparation of a-Si precursor for the μ-Czochralski process on a plastic substrate. The solution based process of Si provided location-control of Si grains with a diameter of 3 μm and the fabrication is still based on vacuum and non-printing process.

In this regards, recrystallization with pulsed, high-power UV lasers, such as excimer-laser, is suited because the heat diffusion is limited to several hundreds nanometers due to the short melt/solidification event in the order of sub-μs, hence the bottom layer won’t be deteriorated [12], [13]. In fact the laser has been applied already for mass-production line of active matrix poly-Si TFTs backplane on a glass for active-matrix flat-panel displays. The problems of the laser crystallized poly-Si film are the small grain size and the dense random grain boundaries, which lowers channel mobility significantly. However, if the location of the silicon islands is controlled, the position of the channel region of FETs can also be aligned inside the island. The 2D location control of Si grains can therefore eliminate inclusion of the random GBs and enables formation of single-grain (SG) TFTs.

2. Single-Grain Si TFTs

Formation of high quality silicon layer with a low-temperature process is a key challenge for realization of the both monolithic 3D-ICs and high-speed flexible electronics. Here the low-temperature process temperature is required to yield no thermal damage to the underlying device layer or plastic substrate. In this regards, recrystallization with pulsed, high-power UV lasers, such as excimer-laser, is suited because the heat diffusion is limited to several hundreds nanometers due to the short melt/solidification event in the order of sub-μs, hence the bottom layer won’t be deteriorated [12], [13]. In fact the laser has been applied already for mass-production line of active matrix poly-Si TFTs backplane on a glass for active-matrix flat-panel displays. The problems of the laser crystallized poly-Si film are the small grain size and the dense random grain boundaries, which lowers channel mobility significantly. However, if the location of the silicon islands is controlled, the position of the channel region of FETs can also be aligned inside the island. The 2D location control of Si grains can therefore eliminate inclusion of the random GBs and enables formation of single-grain (SG) TFTs.

2.1 Location-Control of Si Grains

So far very few have been reported the 2D location control of Si grains and formation of TFTs inside those. Among them the μ-Czochralski (grain-filter) process [15], [16] has advantages in terms of the wide energy density window for obtaining the 2D location control, and the higher alignment accuracy over the other methods. As shown in the Fig. 1, the process can grow large Si grain from “grain filter”, which refers hole created in the underlying SiO2 and filled with a-Si. Upon excimer-laser irradiation, the Si film surrounding the grain-filter melts completely, whereas the grain filter won’t melt completely due to the large heat dissipation and heat capacitance there. At the end of the laser pulse, residual solid at the bottom, consisting of fine poly-Si grains, will subsequently seed grain growth. Even if more than one seed remain in the Si column, a single-grain is expected to be filtered out during the vertical growth along the Si column, because of the competitive grain growth. By increasing the aspect ratio of about more than 7, only single grain can be filtered out from the many pre-existing fine grains. The grain size can be up to 9 μm with optimization of the geometrical structure [14].

The process starts with formation of location-controlled Si grain with the μ-Czochralski process. Experimental details for forming the grain-filter structure has been described elsewhere [17]. First we fabricated narrow cavities (grain-filters) with a diameter and a depth of 100 nm and 200 nm, respectively, by partially filling holes with a diameter of 1 μm made inside 1-μm-thick SiO2 layer on bulk-Si wafer by depositing 2nd SiO2 with PECVD. After deposition of 250 nm thick a-Si by LPCVD at 550°C, a single pulse of XeCl excimer-laser (308 nm, 24 ns) irradiated the structure with a substrate temperature of 450°C. The laser beam has top-hat shape and a size of approximately 3×2 mm, i.e., uniform light exposure for the grain-filter structure. It should be noted that the Si wafer was used for process simplification, and a glass wafer can be used as an alternative substrate. If the sputtering or evaporated a-Si is used, a plastic substrate could also be used.

Figure 2 shows SEM images of the location-controlled Si grains with different spacings between the grain-filters. An array of circular shaped Si grains with a diameter of 8 μm was successfully grown on the predetermined positions of the grain filter. Grain size is determined by the spacing and, when the spacing is shorter than 8 μm, the grains are forced to collide with each other and form a grid of square-shaped grains as shown in the Fig. 1 which has the spacing of 3 μm. Some of the grains have the planar defects which are generated either from the center of the film or from the rim of...
2.2 Crystallographic Orientation Control

It is well known that electronic properties of MOSFET have a pronounced dependence on the orientation due to the effective mass anisotropy [21]. Device performance and uniformity could therefore be improved further by controlling the crystallographic orientation. We succeeded to control the crystallographic orientation of the location-controlled Si grains by combining the metal-induced lateral crystallization (MILC) and the \( \mu \)-Czochralski process [22]. Figure 3 shows the process scheme for the orientation control. First, crystallographic orientation controlled, i.e., textured poly-Si is formed by the MILC of the a-Si using nickel (Ni) as a catalyst. The textured poly-Si are formed behind the propagating NiSi\textsubscript{2} tip which proceeds laterally from the Ni pattern. The growth will continues seamlessly into the grain-filter and then the textured seeds are formed in the grain-filter. To avoid contamination of Ni, the textured poly-Si of only on the surface is removed while keeping the poly-Si inside the grain-filter. Then a new a-Si layer is deposited on top.

Upon irradiation of the excimer-laser, a large grain with a controlled orientation will be obtained by epitaxial growth from the textured and unmelted MILC grown grains at the bottom of the grain filter. Random grain boundaries between the needle-like grains will be filtered out during the vertical growth.

Detailed experiential conditions can be found in elsewhere and here we only describe it shortly [22]. After formation of the grain filter and deposition of 250 nm a-Si film, a 300 nm thick SiO\textsubscript{2} was deposited by PECVD as a capping layer and window was opened. Thin Ni film (10 nm) is then sputtered in the window, the wafer was pre-annealed at 450\(^\circ\)C. After unreacted Ni and SiO\textsubscript{2} were etched away by a wet chemical, the sample was further annealed at 600\(^\circ\)C for 4 hours. During this time, NiSi\textsubscript{2} changes into NiSi\textsubscript{2} and MILC poly-Si has formed. We are able to obtain the surface orientations of \{110\} and \{110\} of the MILC poly-Si grown from the side and the corner of the Ni pattern, respectively. Using those (100) and (110) MILC poly-Si seeds inside the grain filter, the \( \mu \)-Czochralski process has been performed. We then removed the textured poly-Si layer on the surface by a dry-etching. Then a new, 250 nm-thick a-Si layer is deposited on top by LPCVD.

Figure 4 shows SEM and pole-figure obtained by EBSD of the location-controlled grains after the laser irradiation. It can be seen that \{100\} and \{110\} surface oriented grains with a diameter of 6\( \mu \)m grew epitaxially from the seeds at predetermined positions. It should be noted that the in-plane orientations were also controlled successfully as can be seen from the pole-figure.

2.3 TFT Fabrication and Characteristics

Transistors were fabricated inside a single, location-controlled grain. After etching the Si into islands, we deposited a 30 nm-thick TEOS PECVD SiO\textsubscript{2} at 350\(^\circ\)C as a gate insulator. Then Al is deposited and patterned as gate with a gate length of 1.5\( \mu \)m. Source, drain and the gate re-
gions are heavily implanted by either phosphorous or boron ion and activated by the excimer laser with an energy density of 300 mJ/cm². Subsequently 1.2µm thick SiO₂ was deposited and followed by a 2nd contact hole formation to reach the bottom and top devices with the same etching depth. Finally Al was sputtered at 350°C and patterned to form interconnection and pads. The SG Si TFTs exhibit mobility of 600 cm²/Vs and 280 cm²/Vs for electrons and holes, respectively [23]. An operational amplifier was demonstrated with a DC gain of 55 dB and a cutoff frequency of 5.5 GHz for the SG TFTs with the 1.5µm long gate enabled a low-noise RF amplifier operating 433 MHz with 12 dB gain [24].

Using the orientation-controlled grains, these motilities were increased even more. The [100] SG-TFTs show electron mobility of 998 cm²/Vs, while the [110] SG-TFTs show hole mobility of 429 cm²/Vs. In fact the mobility of the [100] SG Si TFTs is higher than that of SOI-TFT that were fabricated with [100] SOI wafer and the same process [22]. This is because of effective mass reduction due to the tensile strain inside the grain induced by the large difference in the heat expansion coefficient between Si and SiO₂.

3. Monolithic 3D-ICs

In this section we will explain design and electrical characteristics of basic circuit building blocks using two single-grain Si TFT layers. Those are CMOS inverters, photodiodes with in pixel amplifiers and 6T SRAM.

3.1 3D CMOS Inverters

We have stacked two SG-TFT layers on top of each other separated with an inter-layer dielectric (ILD) of SiO₂. The schematic of the 3D-ICs is shown in Fig. 5. The fabrication of the bottom layer is the same as the process described above, except the gate electrode of doped-poly-Si, which was crystalized and activated during the S/D activation by excimer-laser. After completing the devices in the first layer, a 1.6µm-thick isolating SiO₂ layer was deposited by PECVD using TEOS. Next step was planarization of the surface using CMP. We polished down around 550 nm oxide to get rid of unsmoothed surface. The fabrication process of the second layer was the same as first layer. We used Al as the gate material for the top layer devices. After making the top gate, we used a 1st contact-hole mask to reach the source, drain and gate of the bottom devices and after deposition of a 1.2µm thick SiO₂ layer, the 2nd mask opened those contacts to the both top and bottom devices. A 3µm-thick-Al deposition at 350°C completed the 3D-IC fabrication.

Figure 6 shows a cross-sectional TEM image of the fabricated CMOS inverters with two SG-TFT layers having the nMOS on top of the pMOS. The cross section is made along the gate width direction. The width of the pMOS is 4.2µm, twice of the nMOS. The gate length of both transistors is 1.5µm. The single-grain channels, the poly-Si gates on the both bottom and top layers, and the common connection between them can be clearly seen.

We first characterized transistor characteristics of the fabricated bottom and top SG-TFTs. Figure 7 shows transfer characteristics of the bottom (a) and top (b) SG TFTs of the both nMOS and pMOS, respectively. A good matching of the transfer characteristics between the top and bottom transistors is observed. Table 1 summarizes the average characteristic values for different devices on each layer. Mobility values were estimated from extracted mutual conductance (gₑₘ) from the Iₑ − Vₑ curves when biased in the linear regime with a drain voltage of 0.2 V. Field-effect mobilities for the top layers are 600 and 200 cm²/Vs and bottom layer mobilities are 400 and 150 cm²/Vs, for the nMOS and pMOS, respectively, as shown in Table 1. The output characteristics of the CMOS inverters are
Table 1  TFT properties of the two SG-TFT layers.

<table>
<thead>
<tr>
<th>TFT type</th>
<th>μ (cm²/Vs)</th>
<th>Vth (V)</th>
<th>S (mV/decade)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Top-nMOS</td>
<td>600</td>
<td>0.5</td>
<td>180</td>
</tr>
<tr>
<td>Top-pMOS</td>
<td>200</td>
<td>−1.7</td>
<td>190</td>
</tr>
<tr>
<td>Bottom-nMOS</td>
<td>400</td>
<td>−0.5</td>
<td>250</td>
</tr>
<tr>
<td>Bottom-pMOS</td>
<td>150</td>
<td>−1.0</td>
<td>240</td>
</tr>
</tbody>
</table>

Fig. 8  Output characteristics of the 3D CMOS inverters with the SG Si TFTs with pMOS on top of nMOS (a) and the reverse configuration (b).

also shown in the Fig. 8. Two different CMOS configurations have been made: one with pMOS on top of nMOS and the other nMOS on top of pMOS. For both types, switching voltage of the inverters lies around 2 V. The input signal swings from 0 to 5 V, and so does the output. The first type shows slightly better inverter characteristics. The inferior inverter characteristic of the nMOS on pMOS is due to the larger leakage current of the nMOS at a high $V_d$.

3.2 Photodiode with In-Pixel Amplifier

The image-sensor that were made in this study is an active pixel sensor (APS) consisting of an array of sensor, each pixel consisting a lateral PIN photodiode fabricated on top of three transistors acting as in-pixel amplifier. As shown in Fig. 9(a), the intrinsic region of the lateral photodiodes having a size of $2 \mu$m/$6 \mu$m of length/width is made inside a single grain. The single-grain PIN photodiode is expected to have a high photo-sensitivity, because of absence of the random GBs, which recombine photo-generated carrier and generates carrier in the dark current. In the design, the large squares are contact holes for access to the P and N regions of the photodiodes. Under the SG photodiode layer, three SG TFTs (reset, source-follower, select transistor) were designed for the in-pixel amplifier for readout, as shown in Fig. 9(b). Every photodiode is connected to three transistors at the bottom layer to convert the photo-generated current to a voltage.

First we characterized light sensitivity of the lateral PIN photo-diode inside a grain. The photodiodes were interdigitated and have the total area of intrinsic region of $36 \mu$m². Upon irradiation of white light, the I-V curve (Fig. 10(b)) of the SG lateral PIN photodiode shows more than 100 times increase of current in the reverse bias regime, which is about 10 times larger than that using poly-Si (Fig. 10(a)), made for a reference purpose. The high sensitivity is because of absence of the random GBs which recombine generated carriers. Quantum efficiency was estimated to be as high as 60% at a wavelength of 310 nm.

Similar photo-sensitivity has been obtained also for a photodiode with the standard 2D process.

Figure 11 shows a transient response of one pixel with the lateral PIN photodiode with the in-pixel amplifier with three SG-TFTs. Frequency of applied pulses (blue line) to the reset signal was 100 Hz with 10% dutycycle. As shown in this figure the output voltage (orange line) of one pixel drops and eventually diminishes within 10 ms. We have obtained an operation frequency of 100 Hz which is fast enough for application to artificial retina.
3.3 3D 6T-SRAM

In the conventional six transistor (6T) SRAM structure, two cross coupled CMOS inverters as a positive feedback to store a value and two access transistors are used for reading and writing the data. Disadvantage of the SRAM is that each cell occupies a lot of area with the conventional 2D-IC configuration. We have designed and fabricated the 6T SRAM cells with two SG Si TFTs. As shown in Fig. 12, two pMOS transistors of the cross-coupled inverter are located on the top of four nMOS transistors, of which two act as access transistor. Because of the vertical stacking, the 3D SRAM cell provides much smaller footprint than that of 2D. The cell area was reduced from 280F^2 to 128F^2 with the channel length of 1.5 µm. In addition, the specific combination can skip doping selection mask step for the S/D as each layer has only one kind of dopant of n- or p-type. This helps a lot in shortening the process time and improving the yield in the fabrication. The fabricated die had a dimension of 10 × 10 mm^2 for both the SRAM and the image sensor.

We have characterized electrical property of the fabricated 6T SRAM with the two layer SG-TFTs. Figure 13 shows a butterfly curve of the fabricated 3D-SRAM. The curve shows that metastable point is almost at the middle of curve owing to the symmetric properties of n- and p-MOS SG TFTs. Read and write SNM (static noise margin) were 0.75 V with a supply voltage of 5 V.

4. Flexible Electronics

Flexible transistors on a plastic substrate are attractive in their applications, not only for flexible displays, but also for implantable wireless sensors. Because of this, organic and metal oxide semiconductors such as IGZO, are researched intensively for TFTs [7], [8]. The devices can be printed without using a vacuum environment, which enables low-cost production. However, the both have mobilities much lower than Si, and for the metal oxide it is not possible to make CMOS devices due to the extremely low hole mobility.

Printing of silicon, however, will provide high carrier mobility and at the same time the possibility of fabricating NMOS and PMOS TFTs in the same process on a large area substrate. In this section we will review our achievements in single-grain Si TFT fabrication on a plastic substrate based on solution process of silicon.

4.1 Liquid-Si

Liquid-Si, which is a UV irradiated cyclopentasilane (CPS) solution with a solvent, enabled solution processing of poly-Si [25]. The CPS is a cyclic-compound having only Si and H atoms (SiH10) as shown in the chemical structure of Fig. 14 and it is transparent liquid at room temperature. The boiling point of 194°C of CPS can be increased by introducing polymeric hydrogenated polysilanes, -(SiH2)n-, which increases the molecular weight. Shimoda, et al., have applied photo-induced ring-opening polymerization to obtain pure hydrogenated polysilanes from the CPS.

By diluting the solution with an organic solvent, such as toluene, they obtained the solution, which is referred to as liquid silicon. When the spin-coated liquid-Si layer is heated in oxygen free environment, organic solvent and CPS evaporate first and then at around 300°C a three-dimensional Si network is formed and a-Si can be obtained. After forming a-Si by sintering spin-coated liquid-Si at 430°C followed by de-hydrogenation, poly-Si TFTs have been fabricated with excimer-laser crystallization. Although mobilities of the resultant TFTs are much superior to those of organic and metal oxide TFTs, the dehydrogenation process with a temperature of more than 550°C is not suitable for polymeric substrates. The mobility of poly-Si is limited by the carrier

![Fig. 12](image12.png)  A 3D view of a 6T SRAM cell when top transistors are pMOS and bottom transistors are nMOS.

![Fig. 13](image13.png)  Butterfly curve of 3D 6T SRAM cell using the two SG Si-TFT layers.

![Fig. 14](image14.png)  Chemical structure of CPS and preparation process for the liquid-Si.
scattering at the grain boundaries.

4.2 Fabrication Process

We have fabricated single-grain Si TFTs by applying the liquid-Si into the $\mu$-Czochralski process. We have also succeeded in lowering the process temperature to 350°C.

As shown in Fig. 15, first, a quasi-plastic substrate is prepared with spin-coating 10-$\mu$m-thick polyimide layer on top of a supporting crystalline Si substrate, which is subsequently cured at 400°C. Then, by the $\mu$-Czochralski process, grain-filters (100 nm diameter and 750 nm depth) are made in 4-$\mu$m-thick SiO$_2$ deposited by plasma-enhanced chemical vapor deposition (PECVD) of (TEOS) at 350°C on the substrate, on which pure CPS (without solvents) is coated using a Si$_3$N$_4$ doctor-blade in a low oxygen-level environment ($< 10$ ppm). To polymerize the layer and increase the boiling point, the coated CPS is irradiated with UV lamp for 20 minutes. Then the polysilane layer was transformed to a-Si film with a thickness of 100 nm by a 1-hour thermal treatment at 350°C on a hot plate in the same environment. This temperature is lower than the 430°C reported in previous studies.

Figure 16(a) shows the cross-section of a grain-filter completely filled with the a-Si. Figure 16(b) in show Raman spectroscopy of the layer. The broad peak at around 480 cm$^{-1}$ indicates that the film was converted into a-Si. Hydrogen concentration in the layer is measured to be 13 at% by Elastic Recoil Detection (ERD).

For crystallization of the a-Si film, a XeCl excimer-laser (308 nm, 250 ns) is employed. To avoid Si eruption due to hydrogen effusion during the laser irradiation [11], the sample is dehydrogenated by laser annealing using the same laser with multiple shots at lower energies. During the laser, the energy density is gradually increased from 300 mJ/cm$^2$ to 900 mJ/cm$^2$ with steps of 50 mJ/cm$^2$, while the number of shots for each energy density is decreased from 100 to 1 with a step of 10 shots. After laser annealing until 500 mJ/cm$^2$, the peak hydrogen concentration decreases from 13 at% to 10 at%, while at the surface, the concentration decreases to 3 at%. After the dehydrogenation, the a-Si film is crystallized by the excimer-laser at room temperature with an energy density of 950 mJ/cm$^2$. Si grains are created on predetermined positions of the grain-filters with a maximum grain size of 3 $\mu$m, as can be seen in Fig. 17.

4.3 TFT Characteristics

TFTs are fabricated inside the grain with a process similar to as described in [23]. After forming Si islands by patterning the Si film, 40 nm gate SiO$_2$ is formed by ICP oxidation.
at 250°C and additional SiO₂ deposited by PECVD-TEOS at 350°C. After that the Al gate is deposited and patterned, source and drain regions are ion-implanted with boron and phosphorus using self-alignment by the gate. The impurities are activated by the excimer-laser. To prevent thermal damage to the polyimide substrate from the laser, an Al layer covers the area outside the gate, source and drain. Passivation SiO₂ deposition at 350°C by PECVD TEOS and contact hole and Al pad formations complete the TFT fabrication. Channel length and width are both 1 µm. Finally, the polyimide substrate is etched away using oxygen plasma. The TFTs can now be peeled off from the crystalline Si wafer by an acrylic-based dicing tape and transferred to a 125 µm thick flexible PEN foil using a glue made of polymers, as shown in Fig. 18. The transfer process is not necessary and the TFTs could be directly fabricated on the polyimide foil as the maximum process temperature was below 350°C. We have introduced the transfer process just because of the ease of handling and processing in our lab if the crystalline-Si substrate was employed as a carrier.

Figures 19 and 20 show the transfer and output characteristics of the NMOS and PMOS TFTs. The carrier mobility estimated in the linear region with a low drain voltage is 460 cm²/Vs and 121 cm²/Vs for electrons and holes, respectively. Table 1 summarizes the device characteristic values. The mobilities are much higher than those of the organic (0.5 cm²/Vs, [6]) and metal oxide (10 cm²/Vs, [8]) TFTs on a plastic substrate. The values are higher than poly-Si TFTs (50 cm²/Vs, [11]) as well because of the absence of the random grain-boundaries inside the channel. The leakage current is below 0.1 pA/µm, which is lower than that of the poly-Si TFTs and suitable for display application. Figure 20 shows the output characteristic of the CMOS inverter, with a full output swing (4.981 V out of 5 V) and with V$_{TH}$ of 2.14 V. Table 2 presents the summary of the inverter characteristics.

After being peeled off with dicing tape and transferred to the flexible foil, the circuit still shows functioning transfer characteristics of NMOS and PMOS TFTs, as shown in Fig. 19. The NMOS TFTs before and after being peeled off are measured on the same transistor, which also applies for PMOS TFTs and inverters. The estimated carrier mobility is 310 cm²/Vs and 110 cm²/Vs for electrons and holes, respectively, which is lower than before they were peeled off. The leakage current of NMOS transistors at high negative gate voltage decreases comparing to that before peeled off. The reason of the reduced carrier mobility is assumed to be the mechanical stress caused by the transfer process and/or stress during the measurement since the substrate is not rigid. The leakage current at V$_{g}$ = −5 V becomes lower than 1 pA/µm. Figure 21 shows the output curve of the CMOS inverter on the flexible foil, with a V$_{TH}$ of 1.50 V, a full output swing (4.981 V out of 5 V), and less-balanced noise margin compared to before being peeled off, since the threshold voltage of both NMOS and PMOS TFTs shifted to more negative values.

5. Conclusions

We reviewed our recent achievements in monolithic 3D-ICs and flexible electronics based on single-grain Si TFTs that...
are fabricated inside a single-grain with a low-temperature process. Based on pulsed-laser crystallization and submicron sized cavities made in the substrate, amorphous-Si precursor film was converted into poly-Si having grains that are formed on predetermined positions. Using the method called µ-Czochralski process and LPCVD a-Si precursor film, two layers of the SG Si TFT layers with the grains having a diameter of 6 µm were vertically stacked with a maximum process temperature of 550°C. Mobility for electrons and holes were 600 cm²/Vs and 200 cm²/Vs, respectively. As a demonstration of monolithic 3D-ICs, the two SG-TFT layers were successfully implemented into CMOS inverter, 3D 6T-SRAM and single-grain lateral PIN photodiode with in-pixel amplifier. The SG Si TFTs were applied to flexible electronics. In this case, the a-Si precursor was prepared by doctor-blade coating of liquid-Si based on pure cyclopentasilane (CPS) on a polyimide (PI) substrate with maximum process temperature of 350°C. The µ-Czochralski process provided location-controlled Si grains with a diameter of 3 µm and mobilities of 460 and 121 cm²/Vs for electrons and holes, respectively, were obtained. The devices on PI were transferred to a plastic foil which can operate with a bending diameter of 6 µm. Those results indicate that the SG TFTs are attractive for their use in both monolithic 3D-ICs and flexible electronics.

Acknowledgments

References


Fig. 21 Output curve of the CMOS inverter on the flexible foil.
on the single-grain Si TFTs won the best paper award of AMPFD2012.

Physics.

member of the IEEE Electron Device Society, the Society for Information related to the TFT technologies for 3D-ICs and flexible electronics. He is a age sensors, and carbon nanotubes. He is in charge of a number of projects con, monolithic three dimensional integrated circuits (3D-IC) applications.

been focused on printed flexible electronics using solution process of silic-}

From liquid-Si on flexible substrates. Her work

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