The required line speed is expected to exceed 40 Gbps by the late 2010s, and nobody knows how this speed will be possible with electrical interconnects [2].

Optical interconnects with silicon photonics have been expected to solve the bandwidth bottleneck problem with LSI chips and have been investigated by many organizations [1], [3]–[7] because of the intrinsic properties of optical signals, such as wide bandwidth, low latency, low power consumption, and low mutual interference, and because of the industrial advantages of silicon for use in the electronics industry. There have been few reports, however, on inter-chip interconnects that have been made using silicon photonics and that have been fully integrated with light sources, optical modulators, and photodetectors (PDs) on a single silicon substrate.

In this paper, we examine photonics-electronics integration, propose a photonics-electronics convergence system with a silicon optical interposer to solve the bandwidth bottleneck problem in inter-chip interconnects, investigate optical components for the optical interposers, and demonstrate the feasibility of the system by presenting the results of data transmission experiments with the silicon optical interposers.

1. Introduction

The inter-chip bandwidths in personal computers and servers have been doubling every two years [1]. For example, since a CPU for high-end servers has an overall inter-chip bandwidth of about 1.5 Tbps, which consists of 0.5 Tbps for CPU-CPU interconnects (QPI), 0.4 Tbps for CPU-memory (DDR3), and 0.6 Tbps for CPU-peripherals (PCIe 3) at this moment, the overall inter-chip bandwidth is expected to reach a 10-Tbps level by the late 2010s. Although the wiring pitches in logic circuits are expected to shrink exponentially on the basis of Moore’s law, LSI I/O pad pitches, such as flip-chip pad pitches, are expected to remain large [2]. Consequently, the scaling gap between intra-chip and inter-chip is going to widen annually. This is why the line speed for inter-chip interconnects in the future will need to be much higher than that for intra-chip ones. The required line speed is expected to exceed 40 Gbps by the late 2010s, and nobody knows how this speed will be possible with electrical interconnects [2].

OPTICAL INTERCONNECTS WITH SILICON PHOTONICS HAVE BEEN EXPECTED TO SOLVE THE BANDWIDTH BOTTLENECK PROBLEM WITH LSI CHIPS AND HAVE BEEN INVESTIGATED BY MANY ORGANIZATIONS [1], [3]–[7] BECAUSE OF THE INTRINSIC PROPERTIES OF OPTICAL SIGNALS, SUCH AS WIDE BANDWIDTH, LOW LATENCY, LOW POWER CONSUMPTION, AND LOW MUTUAL INTERFERENCE, AND BECAUSE OF THE INDUSTRIAL ADVANTAGES OF SILICON FOR USE IN THE ELECTRONICS INDUSTRY. THERE HAVE BEEN FEW REPORTS, HOWEVER, ON INTER-CHIP INTERCONNECTS THAT HAVE BEEN MADE USING SILICON PHOTONICS AND THAT HAVE BEEN FULLY INTEGRATED WITH LIGHT SOURCES, OPTICAL MODULATORS, AND PHOTODETECTORS (PDs) ON A SINGLE SILICON SUBSTRATE.

In this paper, we examine photonics-electronics integration, propose a photonics-electronics convergence system with a silicon optical interposer to solve the bandwidth bottleneck problem in inter-chip interconnects, investigate optical components for the optical interposers, and demonstrate the feasibility of the system by presenting the results of data transmission experiments with the silicon optical interposers.

2. Photonics-Electronics Convergence System for Inter-Chip Interconnects

2.1 Integration between Photonics and Electronics

Because the performance of electrical interconnects generally declines with their distance more rapidly than does that of optical interconnects, it is important to place optical transceivers (E/O and O/E signal converters) as close to LSIs as possible for wide-bandwidth inter-chip interconnects with photonic wiring. Silicon photonics is the most suitable technology for these applications because of its compactness and compatibility with LSIs.

Generally, there are three types of integration between photonic and electronic circuits with silicon photonics: front-end integration, back-end integration, and flip-chip bonding (see cross sections in Fig. 1). The first two are monolithic integrations and the last is a hybrid integration. Monolithic integration, especially front-end integration, is expected to provide higher speed and lower assembling cost than hybrid integration, but it requires very strict CMOS compatibilities in terms of design, fabrication, and
testing. We think that it will be a long time before the technology is mature enough. On the other hand, the hybrid integration allows us to choose the most suitable technology nodes separately for photonics and electronics circuits, to design, fabricate and test them separately, and then combine their good dies. This scheme can improve product yields and stimulate horizontal specialization between electronics and photonics, or between LSI chips and their inter-chip interconnects. Therefore, since we think that the hybrid integration is the most practical choice now and in the near future, we have taken the hybrid-integration route to photonic-electronic integration for inter-chip interconnects.

2.2 Light Source Integration

Considering light source arrangement in optical inter-chip interconnects, we had first to choose off-chip sources or on-chip sources. Although the off-chip light sources are more flexible than the on-chip ones, they require highly precise optical connectors to get optical power from the off-chip light sources into the substrate. Because we think that these optical connectors are not practical for large scale interconnects, we have chosen on-chip light sources. There are two types of integrations for on-chip light sources: monolithic integration with silicon or germanium lasers, and hybrid integration with compound semiconductor lasers. Monolithically integrated Ge-on-Si lasers were recently reported [8], but their efficiency and output optical power are low for inter-chip interconnects applications. We have therefore chosen hybridly integrated lasers for inter-chip interconnect applications.

2.3 Conceptual Model

The conceptual model of the photonics-electronics convergence system for inter-chip interconnects is outlined in Fig. 2. The upper-left LSI chip on the silicon optical interposer has been removed to enable the substrate surface area that it covered to be seen. Optical splitters, optical modulators, and PDs are monolithically integrated on a silicon substrate, arrayed LDs are hybridly integrated on the substrate, and these optical components are optically linked to each other via silicon optical waveguides. Together they form a silicon optical interposer. Bare LSI chips are mounted on the interposer and are electrically connected to the optical modulators and PDs by flip-chip bonding. That is, electric circuits (the bare LSI chips) and photonic circuits (the optical interposer) are integrated hybridly.

The inter-chip interconnects with the silicon optical interposers operate as follows. Arrayed LDs are driven simultaneously by DC current. The CW light from each LD is divided by an optical splitter and launched into an optical modulator. The optical modulators are directly driven by transmitter circuits in one LSI. The modulated optical signals propagate along inter-chip optical waveguides and are the input for PDs under another LSI. The electrical signals from those PDs are the input for receiver circuits in the LSI that the PDs are under.

This system enables us to replace the conventional electronic wires on a printed circuit board (PCB) with the optical interconnects on a silicon substrate, which is one hundredth the size of a PCB. This silicon optical interposer has wide bandwidth capabilities due to the properties of its optical signals. Since the silicon substrates can be fabricated using a CMOS-compatible process, they have quite high density and are low in cost. Furthermore, because this system is optically complete and closed without any optical inputs or outputs, users do not have to worry about any op-
tical issues, such as optical coupling, optical reflection, or polarization dependence.

3. Configurations and Characteristics of Optical Components

To demonstrate the feasibility of the photonics-electronics convergence system, we fabricated a high-density silicon optical interposer that mainly consisted of silicon optical waveguides, silicon optical modulators, germanium PDs, LDs, and spot-size converters (SSCs) between the LDs and the silicon optical waveguides. Configurations and characteristics of these optical components were investigated as follows.

3.1 Silicon Optical Waveguides

Generally, there are two types of silicon optical waveguides in terms of their core cross section shapes: rib-shaped and rectangular. The propagation loss of the rib-shaped waveguides is lower than that of the rectangular ones, but the rib-shaped waveguides pose difficulties in the fabrication process in that we have to stop etching the silicon layer to leave a precisely thin silicon slab. We think this issue is critical in terms of yields in mass production, especially, as will be explained later, for the yields of optical modulators. We have therefore chosen rectangular core waveguides for our silicon optical interposers, and we have developed fine lithography and etching processes in our clean room for rectangular core waveguides. As a result, with a rectangular core that was 480-nm wide and 220-nm thick we have obtained propagation losses as low as 4 dB/cm at a 1530-nm wavelength.

3.2 Silicon Optical Modulators

There were a lot of research activities regarding silicon optical modulators using the carrier plasma effect in PIN or PN diode [11]–[13], and most of them used a doped silicon slab in the rib-shaped waveguides to make electric contact between their waveguide core and metal electrodes. In these cases, the gap between P- and N-doping areas should be wider than the width of the optical mode profile to prevent optical absorption loss due to the highly doped carriers. The optical mode profile in these rib-shaped waveguides extended to the slab area, and a thicker slab caused a wider mode profile and P–N gap. The wider P–N gap made the resistivity higher and made the modulation efficiency and modulation speed lower. Because optical modulator characteristics such as optical loss, modulation efficiency, and speed were sensitive to the slab thickness in this way, we had to stop etching the silicon layer to leave a precisely thin silicon slab.

To overcome these design and fabrication difficulties, we have proposed a novel structure for the electric contact between the waveguide core and electrodes instead of the silicon slab. Figure 3(a) is a schematic of the structure of our proposed optical modulators [14]. The optical modulator is a Mach-Zehnder (MZ) interferometer composed of phase shifters and multimode interference (MMI) couplers. The phase shifters, which have side-wall gratings on both sides of the waveguide core in order to enable electric contact between the core and metal electrodes, can change their refractive indices by the carrier plasma effect in lateral PIN diode structures. Figure 3(b) shows microscope and SEM images of the fabricated modulator. Because the waveguides had a uniform thickness of silicon over the entire modulator, the etching process was much easier than that with rib-shaped waveguides. Moreover, this structure enabled stronger lateral optical mode confinement, a narrower optical mode profile, a narrower P–N gap, lower resistivity, higher efficiency, and higher speed than the modulators with rib-shaped waveguides. The pitch of the side-wall grating was designed so that the stop-band wavelength was much shorter than the operation wavelength. The interaction length of the phase shifter was 250 μm.

The measured DC response of the optical modulator is plotted in Fig. 4. The π-phase shift voltage (Vπ) was 0.13 V and the modulation efficiency (Vπ*L) was 0.003 Vcm, which is four times as high as the efficiency of our previous modulator with rib-shaped waveguides [7]. The extinction ratio (ER) was 14.3 dB.

3.3 Germanium Photodetectors

There are generally two types of germanium PDs that we can monolithically integrate on a silicon substrate: PIN-PDs and metal-semiconductor-metal (MSM) PDs. MSM-PDs require fewer fabrication steps but finer patterning and alignment than PIN-PDs. In this work we fabricated MSM-PDs for the silicon optical interposers. Figure 5(a) is a
schematic of the structure of our germanium MSM-PD [15], and Fig. 5(b) also shows microscope and SEM images of it.

The measured frequency responses of PDs with 4- to 10-V biases are plotted in Fig. 6. The 3-dB cutoff frequencies were 6 GHz with a 4-V bias voltage and 9 GHz with a 10-V bias voltage. The dark current of the PDs was about 1 μA. The photo to dark current ratio was higher than 30 dB. The responsivity was 1 A/W.

3.4 Arrayed Laser Diodes

The LD chip was a 13-channel InGaAsP LD array with a 30-μm channel pitch. Each channel was a Fabry-Perot type LD with a spot-size converter. The chip had a single pair of electrodes for all 13 channels, which simultaneously emitted 1550-nm light. The near field pattern and output intensity of the 13-channel LD array are shown in Fig. 7. The output power uniformity across all the channels was better than 0.7 dB.

3.5 Spot-Size Converters

Spot-size converters between the LDs and silicon optical waveguides are key components for the silicon optical interconnectors in terms of their optical power budget and fabrication process simplicity. We previously had two types of SSC: tapered silicon waveguides and SiON waveguides. The former did not need additional processes but had large coupling loss [7], and the latter had low coupling loss but needed additional processes [10]. We later introduced a novel SSC called a trident [16]. The schematic structure and SEM images of the trident SSC are shown in Fig. 8. It consists of only three narrow silicon waveguides fabricated without additional process. Measured coupling losses between the LD and the trident SSC with various alignment deviations in the
horizontal and vertical directions are plotted in Fig. 9. We obtained coupling losses as low as 2.3 dB, and the alignment error tolerance up to 1-dB loss increase was about ±0.9 μm in both directions, which was large enough for our alignment precision (±0.5 μm) with a passive alignment technique [17].

4. Fabrication of Silicon Optical Interposers

The silicon optical interposers were fabricated from 4-inch silicon-on-insulator (SOI) wafers in the Super Clean Room at AIST Tsukuba West by using CMOS process technology. The silicon optical waveguides were formed by electron-beam lithography and dry etching. The epitaxial germanium mesas for the PDs were selectively grown on the silicon waveguide by chemical vapor deposition. The waveguides, modulators, and PDs were covered with the SiO₂ upper cladding layer by chemical vapor deposition. The waveguide endfaces and the pedestals for the LD mount were formed by dry etching. An arrayed LD chip was hybridly integrated on the substrate with a passive alignment technique [17]. As a result, the LD array was butt-coupled to the silicon waveguide array via the trident SSC array. The I-L characteristics of the LDs measured without temperature control are plotted in Fig. 10, where the blue line shows the I-L characteristics of the 13-ch. arrayed LD hybridly integrated on the interposer and the red line shows that of a 1-ch. LD on a heat sink. Since all 13 channels were driven simultaneously, the actual current injected into the arrayed LD chip was 13 times of the value in the horizontal axis. Although the heat generation in the 13-ch. LD was 13 times as high as that in the 1-ch. LD, both I-L characteristics had about the same threshold currents and slope efficiencies, and no output power saturations up to 10 mW or more per channel. That suggests this hybridly integrated arrayed LD had a quite high heat dissipation capability. We think that the high output power and high heat dissipation capabilities are advantages of our butt-coupled hybrid lasers over evanescent-coupled ones.

Figure 11 shows a photograph of a silicon optical interposer fabricated on a 5 mm × 5 mm substrate. A trident SSC array, a 1 × 4 optical splitter, an optical modulator array, and a PD array were monolithically integrated on a single silicon substrate, and a 13-channel arrayed LD chip was hybridly integrated on the substrate. These optical components were optically linked to each other via a silicon optical waveguide array.

5. Data Transmission Experiments

Data transmission experiments with the silicon optical interposers were carried out as follows. All 13 channels of the arrayed LD were simultaneously driven by a single DC current. The CW light from the LD was divided into four by the 1 × 4 optical splitter and each of them launched into the optical modulator. RF input signals were pre-emphasized by a differentiator consisting of passive RC circuits and were modulator input. The voltage amplitude after pre-emphasis was 3.4 V peak to peak. The modulated optical signals propagated along the optical waveguides and were led to the PD array, which converted them into electrical signals.

The measured eye diagram of PD output at 12.5-Gbps NRZ with a 27-1 pseudo-random binary sequence (PRBS) via 1 × 4 optical splitter is shown in Fig. 12. The clear eye opening suggests that the optical links were capable of data transmission at 12.5 Gbps. The measured bit error rates (BER) for the 12.5-Gbps PRBS are plotted in Fig. 13. We confirmed that BER was less than 10⁻¹² when the PD input power was more than −5 dBm. Error-free data transmission
at 12.5 Gbps via the 1 × 4 optical splitter was achieved. Because this system was optically complete and closed, we did not need to align fibers, control polarization, or control temperature throughout the experiments.

The optical power budget per channel is summarized in Table 1. The optical waveguide length was about 5.3 mm. The overall optical loss was 18 dB, including inherent 6-dB branching loss and 3-dB modulation loss. Because of the novel trident SSC with a quite low coupling loss, we obtained an optical power margin that enabled us to introduce the 1 × 4 optical splitter. These results suggest that integrating a 13-channel arrayed LD, 13 1 × 4 optical splitters, and 52 modulators and PDs enables the optical interposer on a single silicon substrate to achieve a bandwidth of 650 Gbps. Furthermore, we can increase the optical waveguide length to 20 mm by removing the 1 × 4 optical splitters.

The per-channel footprints of the optical components are listed in Table 2. The per-channel footprint of laser diode was also split into four due to the 1 × 4 optical splitter. The total footprint was 0.19 mm² per channel, meaning we could achieve a bandwidth density of 6.6 Tbps/cm² with a channel line rate of 12.5 Gbps. We would like to emphasize that we achieved this high bandwidth density with MZ modulators, which are generally larger but more practical than ring modulators.

Since the typical CPU die is about 2 cm² in area, we can obtain an overall inter-chip bandwidth of 10-Tbps level, which will satisfy the required bandwidth in the late 2010’s as mentioned previously, by using the silicon optical interposers. About two-thirds of the total footprint was occupied by electrode pads in these experiments. And we have already reported individual optical modulators and PDs, which operate faster than 40 Gbps and can be integrated on the silicon optical interposer [18], [19]. Therefore we expect to improve the bandwidth density further with the faster components and smaller pads in the near future.

### 6. Conclusion

We proposed a photonics-electronics convergence system with a silicon optical interposer in order to solve the bandwidth bottleneck problem that inter-chip interconnects have. We examined integration between photonics and electronics and integration between light sources and silicon substrates, and we fabricated a conceptual model of the proposed system based on the results of those examinations. We also investigated the configurations and characteristics of optical components for the silicon optical interposer: silicon optical waveguides, silicon optical modulators, germanium photodetectors, arrayed laser diodes, and spot-size converters. We then demonstrated the feasibility of the system by fabricating a high density optical interposer by using silicon photonics integrated with these optical components on a single silicon substrate. As a result, we achieved error-free data transmission at 12.5 Gbps and high bandwidth density of 6.6 Tbps/cm² with the optical interposer. We think that this technology will solve the bandwidth bottleneck problem.

### Acknowledgments

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**Table 1** Optical power budget.

<table>
<thead>
<tr>
<th>Items</th>
<th>Power (dBm)</th>
<th>Loss (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>LD output power</td>
<td>13.0 dbm</td>
<td></td>
</tr>
<tr>
<td>LD to waveguide coupling loss</td>
<td></td>
<td>2.3</td>
</tr>
<tr>
<td>Inherent 1 × 4 branching loss</td>
<td></td>
<td>6.0</td>
</tr>
<tr>
<td>1 × 4 branching excess loss</td>
<td></td>
<td>0.5</td>
</tr>
<tr>
<td>Inherent modulation loss</td>
<td></td>
<td>3.0</td>
</tr>
<tr>
<td>Optical modulator excess loss</td>
<td></td>
<td>2.8</td>
</tr>
<tr>
<td>Waveguide propagation loss</td>
<td></td>
<td>2.2</td>
</tr>
<tr>
<td>Other losses</td>
<td></td>
<td>1.2</td>
</tr>
<tr>
<td>Total optical power loss</td>
<td></td>
<td>18.0</td>
</tr>
<tr>
<td>PD input power</td>
<td>-5.0 dbm</td>
<td></td>
</tr>
</tbody>
</table>

**Table 2** Per-channel footprints of optical components.

<table>
<thead>
<tr>
<th>Components</th>
<th>Footprints</th>
</tr>
</thead>
<tbody>
<tr>
<td>Laser diode</td>
<td>0.008 mm²</td>
</tr>
<tr>
<td>Optical modulator</td>
<td>0.162 mm²</td>
</tr>
<tr>
<td>Photodetector</td>
<td>0.020 mm²</td>
</tr>
<tr>
<td>Total</td>
<td>0.190 mm²</td>
</tr>
</tbody>
</table>
motion of Science (JSPS) through its “Funding Program for World-Leading Innovative R&D on Science and Technology (FIRST Program).” Part of the fabrication was conducted at the Nano-Processing Facility, supported by IBEC Innovation Platform, AIST.

References


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