SUMMARY 524,288 NbN-based Josephson junctions were integrated to produce a programmable Josephson voltage standard (PJVS) on a die of 15 mm × 15 mm, and the PJVS circuit was cooled to 10 K using a cryo-cooler and operated with a current margin of about 1.0 mA. Although an output voltage of 10 V was required for a voltage standard, the circuit was designed to generate the maximum output voltage of 17 V because it was difficult to avoid a reduction of the output voltage due to defects. Although a perfect chip without any defect was rarely fabricated, the high voltage chip that generated at least 10 V was fabricated with the fabrication yield of larger than 30%. The fabrication yield was also improved by optimizing the film growth conditions to reduce the film stress and the number of particles. Applications for a secondary voltage standard and an ac Josephson voltage standard are also described.

key words: NbN, TiN, SNS, voltage standard, cryocooler

1. Introduction

NbN is a promising material for high-frequency radiation detectors such as low-noise terahertz SIS mixers because it has large gap frequencies of up to 1.4 THz [1], [2]. NbN/Nb oxide/NbN [3], [4] and NbN/MgO/NbN [5] tunnel junctions have been demonstrated for LSI logic circuits. These NbN-based tunnel junctions tend to have relatively high leakage currents, whereas an NbN/AIN/NbN tunnel junction has been demonstrated that has a small leakage current and a high current density for SIS mixer applications [8], [9]. In addition, NbN has a relatively high transition temperature $T_c$, and it is preferable for a phonon-cooled hot-electron bolometer (HEB) superconducting mixer because the IF bandwidth depends on the electron-phonon interaction time, which is temperature dependent [6], [7]. NbN is also promising for voltage standard circuits because it has a high operating temperature, which significantly reduces the size and cost of cryocoolers required to cool the circuits. Hamilton et al. demonstrated a programmable Josephson voltage standard circuit (PJVS) with a binary divided Josephson junction (JJ) array using resistor-shunted Nb/AlOx/Nb junctions [10].

An overdamped junction with non-hysteretic $I$–$V$ characteristics is necessary for D/A conversion; superconductor-normal metal–superconductor (SNS) JJs are preferable to tunnel junctions with external shunt resistors because SNS JJs have small floating inductances and high critical current densities of over 50 kA/cm$^2$ that provide a large operating current margin [11]. PJVS circuits have also been demonstrated with overdamped Nb/AlOx/Nb/AlOx/Nb(SNIS) [12] and Nb/Al-AlOx/Nb (SNIS) [13] junctions. Various normal metals (e.g., PdAu [11], MoSi [14], NbSi [15] and HfTi [16]) have been proposed for Nb-based SNS junctions, whereas metal nitrides (e.g., TiN [17] and TaN [18]) have been proposed for NbN-based junctions. While PJVS circuits with output voltages of over 10 V have been demonstrated with Nb/AlOx/Nb/AlOx/Nb [19], Nb/NbSi/Nb [20] junctions, it is challenges to fabricate such large circuits containing larger than 100,000 JJs with a practical fabrication yield. We have demonstrated a 10-V PJVS circuit using double-stacked NbN/TiN/NbN JJs with a practical fabrication yield of larger than 30% [21].

This paper describes the fabrication and characteristics of an NbN film, an NbN-based overdamped junction, and a JJ array for a voltage standard circuit. It also presents efforts to improve the fabrication yield and the operating current margin. In addition, current under-developed metrological applications are mentioned.

2. NbN-Based Overdamped Josephson Junction

2.1 NbN Film Preparation

Polycrystalline NbN films rather than epitaxial NbN films were used for Josephson voltage standard circuits because many JJs need to be integrated in a relatively large chip area (e.g., 15 mm × 15 mm) and fabrication process for epitaxial NbN films using a 3-inch-diameter wafer has not been established at the AIST.

The NbN films were deposited on a 3-inch-diameter Si wafer by reactive rf-magnetron sputtering using a 6-inch-diameter niobium target in an N$_2$, Ar, and C$_2$H$_2$ gas mixture at ambient temperature without intentional heating. The NbN films were deposited using a total pressure of 2 Pa, an Ar gas flow rate of 52 standard cubic centimeters per minute (sccm), an N$_2$ gas flow rate of 2.7 sccm, and an incident power of 600 W, which gave a deposition rate of 1.3 nm/s. We confirmed the long-term process stability over more than 10 years since NbN films with a critical temperature of about 16 K could be reproducibly prepared at the same N$_2$ flow rate and the same total gas pressure.

The stress in the deposited films was evaluated by esti-
mating wafer bending using Stoney’s equation [22]. In reactive NbN sputtering, the N2 partial pressure determines the critical temperature and the Ar partial pressure mainly influences the intrinsic stress [23], [24]. Films with a high $T_c$ prepared with a low Ar pressure tend to have high film stresses [25]. An NbN film with a high $T_c$ and a low film stress is preferable for large-scale integrated circuits because a high film stress may reduce the fabrication yield due to delamination of the film. Figure 1 shows the N2 flow rate dependence of the critical temperature $T_c$ and the film stress $\sigma$ sputter deposited using different Ar flow rates. The film thicknesses are about 200 nm. This result suggests that using higher Ar gas flow rate reduces the film stress. It is also found that the N2 flow rate that maximize $T_c$ and that minimize the film stress are equal, as shown by the broken lines in Fig. 1. As a result, a nearly stress-free NbN film with $T_c = 16$ K and $\rho_{20K} = 152.3 \mu\Omega \cdot \text{cm}$ was obtained at a total sputtering pressure of 2 Pa with an Ar gas flow rate of 100 sccm.

2.2 NbN/TiN/NbN Junction

The junctions have an optimum operating frequency $\Omega(=f/I_cR_nK_n) \approx 1$, where $K_n = 483.597.9$ GHz/V, and the greatest tolerance of the step position to critical current variation in arrays is also obtained at $\Omega \approx 1$. Consequently, the product $I_cR_n$ of the junction has to be carefully adjusted by varying the TiN film thickness. Figures 2(a) and (b) respectively show the dependences of the critical current $I_c$ and the normal resistance $R_n$ measured at 10 K on the TiN thickness $d$. The normal coherent length $\xi_n$ is estimated to be about 3.7 nm from the slope in Fig. 2(a) and the equation of $I_c \propto \exp(-d/\xi_n)$. The TiN film was deposited by reactive rf-magnetron sputtering using a titanium target in an N2 gas at the total pressure of 1.33 Pa with the incident power of 600 W. During deposition of the TiN film, the substrate holder was rotated at 10 rpm to improve the uniformity. The TiN film was deposited at a rate of typically 0.02 nm/s. The TiN film had a resistivity $\rho_f$ of 733 $\mu\Omega \cdot \text{cm}$ at 4.2 K, and it varied little in the temperature range of 4 to 300 K. The TiN film may be N rich relative to the stoichiometric composition, and it was dark brown and had a transition temperature of 2.7 K. The resistivity of the TiN film was strongly dependent on the total N2 pressure and the N2 flow rate in an Ar and N2 gas mixture. In contrast, the normal junction resistance $R_n$ was approximately constant; specifically, the normal resistance of the NbN/TiN/NbN junction $R_n$ did not depend on the resistivity of the TiN film. The resistivity $\rho_j$ is estimated to be approximately 318 $\mu\Omega \cdot \text{cm}$ from the slope in Fig. 2(b) and the equation of $R_n = (\rho_j/L^2)d$, where $L = 2.8 \mu\text{m}$ is the junction size; this resistivity is much smaller than that of the TiN film $\rho_f$ measured by the four-probe method. The reason for this discrepancy in the resistivities is unclear; the films were grown on different substrates with different top passivation layers, which may af-
fect the resistivity. Another possible cause is columnar grain growth. Electron scattering from grain boundaries generally dominates the in-plane resistivity, whereas there are no grain boundaries for the vertical resistivity [26].

3. Voltage Standard Circuit

3.1 Design and Fabrication

The National Institute of Advanced Industrial Science and Technology (AIST) and the National Institute of Standards and Technology (NIST) jointly demonstrated a D/A conversion using 4,096 NbN/TiN/NbN JJs and a 10-V PJVS circuit with 327,680 JJs [21]. Figure 3(a) shows the first prototype of the PJVS chip and Fig. 3(b) shows the latest PJVS chip that contains 524,288 JJs. The PJVS chip consists of co-planar waveguides (CPWs), JJ arrays, low-pass filters, dc-block capacitors, microwave termination resistors, and a microwave power divider. They were numerically optimized by an electromagnetic simulator.

Figure 4 shows a cross-sectional view of the PJVS circuit and Table 1 lists its specifications. In the chip, the junction arrays were divided into 64 parallel arrays each containing 4096 double-junction stacks (8192 JJs). A 16 GHz quarter-wavelength CPW with a specific impedance of 36Ω was connected to two 50Ω CPWs, which functioned as two-way splitters. Six consecutive stages of the two-way splitters were connected in series to divide the microwave into 64 arrays. Sixteen cells containing four arrays generate about 1 V each; two of them have binary subarrays with resolutions of 9 bits. The 10 cells having the higher operating current margins were selected from 16 cells to generate a maximum voltage of 10 V; namely, it functions as a decimal DAC and one of the 10 cells with the binary subarrays functions as a 1 V binary DAC to give a high resolution.

The fabrication process for the NbN-based circuit [21] was almost compatible with that for the Nb-based circuit. An AlN film (as an etch stop) and an NbN/TiN/NbN/TiN/NbN multilayer were consecutively deposited by reactive rf-magnetron sputtering on a 3-inch-diameter Si wafer. The TiN barrier was typically thick 24 nm; this thickness was chosen to provide an $I_cR_n$ of 33 μA at 10 K. The NbN counter electrode, two TiN barriers, and an NbN middle electrode were patterned to define Josephson junctions by reactive ion etching (RIE), and the base electrode was subsequently patterned by RIE. The photoresist was removed using an N-methyl-2-pyrrolidone (NMP) jet, which was 0.1 mm in diameter and had a pressure of 8 MPa. To fabricate the termination resistors, a Pd film was sputter deposited and then patterned by the lift-off method. A 400-nm-thick SiO$_2$ film as the electrical isolation was deposited by rf sputtering. Via holes were formed by RIE of the SiO$_2$ layer and a portion of the counter electrodes. A 600-nm-thick NbN film was deposited as a wiring layer. However, because of the previously patterned structures, this NbN film was not flat and had grain boundaries at the step edges. To prevent a significant reduction in the wiring critical current, the surface of the NbN wiring was planarized by chemical-mechanical polishing (CMP). An additional NbN film was deposited on the flat surface and these films were patterned by RIE. Finally, a SiO$_2$ passivation layer was deposited and contact holes were formed to the dc bias pad by RIE.

3.2 Fabrication Yield

There is generally a trade-off between the microwave frequency of the JJ array and the number of junctions to obtain a constant voltage. Since the microwave frequency was 16 GHz, the cost of the microwave source, cables and other components was relatively low. The constant voltage step was relatively small. At this frequency, more than 300,000 JJs are required to generate an output voltage of 10 V, whereas only 70,000 junctions are needed to generate the same output voltage at a frequency of 90 GHz [19]. A large chip area is required to integrate so many junctions, which could significantly reduce the fabrication yield. One way to overcome this problem is to vertically stack JJs; for example, more than 300,000 JJs can be integrated on a sin-
gle die of about 200 mm$^2$ using double- or triple-stacked junctions [20], [21].

There were major and minor defects for the PJVS circuit. A short circuit between the array and the ground and an open or resistive junction across the array are critical defects because they affect a total voltage of the array. On the other hand, missing junctions due to a superconducting bridge between electrodes or a pin hole in the barrier are admissible because it does not generate any voltage. Defects can also damage microwave circuits and reduce the operating current margin. We primarily attempted to reduce the probability of critical defects to fabricate as many available die as possible. A microscopy observation suggested that both short and open circuits are formed by delamination of the insulating layer due to particles, film stress, or contamination. To remove particles and contamination from the wafer, an NMP jet was used to remove the photoresist after patterning by RIE. In addition, the air conditioner in the clean room was upgraded to maintain the relative humidity at about 50%, and eventually water marks due to a dew condensation were prevented from forming on the wafer surface.

We have used an MgO as etch stop layers for many years, but we have neglected to consider that the etch stop layer also contains particles that reduce the fabrication yield. We found that Al or AlN layers contained smaller particles than MgO layers and that the particle density depended on the film deposition conditions (e.g., pressure and incident rf-power). Figure 5 shows the dependences of the particle density in the film deposition on the incident rf power during film deposition. The films were deposited for 300 s; the film thickness was approximately proportional to the rf power. The number of particles in the film was estimated by counting the number of particles in a certain area of a microscopy image; this method was precise enough for qualitative estimation. Fewer particles were formed when the AlN film was sputter deposited at higher incident rf powers and for shorter deposition times.

In addition, we experimentally confirmed that the effective fabrication yield was significantly improved by using a PJVS chip with additional JJs. Although an output voltage of 10 V was required for a voltage standard, the circuit was designed to generate the maximum output voltage of 17 V. The junction array is divided into 16 cells, and dc-bias currents will not be supplied to the cells including minor defects such as a missing junction so that they constantly generate zero volt. Although a perfect chip without any defect was fabricated with the fabrication yield of a few percent, the high voltage chip that generated at least 10 V was fabricated with that of larger than 30%.

3.3 Operating Current Margin

Since the operating current margin of the PJVS is determined by both the zeroth ($n=0$) and first $n=1$ constant voltage steps and since the $n=0$ step is typically much larger than the $n=1$ step, we discuss the operating current margin in terms of the $n=1$ step. The double-barrier JJ reduced the chip area and increased the number of dies on a wafer, which lowered the cost and increased the fabrication yield. Figure 6 shows a plot of the secular change in the difference between the $I_c$ of the upper and lower junctions over about 5 years. It suggests that this difference is smaller than 15% up to about 1 year after exchanging the Nb target and it exceeds 30% after about 1 year. Therefore, we exchanged the Nb target after 100 elapsed hours even if the Nb target was still thicker than half of the Nb target. Figure 7 shows the relation between the normalized $n=1$ Shapiro step height and the difference in $I_c$ for the upper and lower junctions $\Delta I_c$; it was numerically calculated using the resistively shunted junction (RSJ) model [27]. For simplicity, the variation in $R_n$ was not taken into account. A difference in $I_c$ of 15%, which is experimentally observed in typical double-barrier junctions, suppressed the current margin by about 20%, while a difference in $I_c$ of 40% suppressed the margin by about a factor of two. These results suggest that a difference in $I_c$ for the upper and lower junctions of about 15% does not critically affect the practical operating current.

![Fig. 5](image1.png) Fig. 5 Dependence of particle density in an AlN film on incident rf power during film deposition.

![Fig. 6](image2.png) Fig. 6 5-year secular change in the difference in $I_c$ for the double-barrier junctions sputter deposited using different Nb targets.
Fig. 7  Numerically calculated $n = 1$ Shapiro step height as a function of the difference in $I_c$ between the upper and lower junctions.

Fig. 8  Dependence of the $n = 1$ step height on the number of JJs. Closed circles and triangles show measured step heights and closed and broken lines indicate numerical calculation results using the RSJ model for different variations in $I_c$.

The applied microwave power decreased rapidly in the dissipative junction array. The microwave power at the end of the array $P_{\text{end}}$ is given by $P_{\text{end}} \propto \exp(-R_nN/Z_0)$, where $R_n$ is the junction resistance, $N$ is the number of JJs, and $Z_0$ is the characteristic impedance of the array. The $n = 1$ Shapiro step height $I_{s1}$ is expressed by the Bessel function $J_1(v_{\text{end}})$ as a function of the microwave voltage $v_{\text{end}}$ when biased with a current source. When the microwave voltage $v_{\text{end}}$ is sufficiently small to use the approximation $J_1(v_{\text{end}}) \propto v_{\text{end}}$, the $n = 1$ Shapiro step height $I_{s1}$ can be approximated by

$$I_{s1} \propto \exp\left(-\frac{R_n}{2Z_0}N\right) \quad (1)$$

This is a simple qualitative approximation. For a quantitative investigation, a numerical simulation using the RSJ model was performed. Figure 8 shows the dependence of the $n = 1$ step height on the number of JJs. The solid and broken lines indicate step heights numerically calculated using the RSJ model for different variations in $I_c$, and the closed circles and triangles show the experimentally measured values. Since the variation in $R_n$ was not taken into account in the calculation, the calculated step heights were larger than the measured ones. The effect of the Josephson penetration depth was not taken into account, which could account for the discrepancy between the measured and calculated values for small $N$ and large $I_{s1}$.

Figure 9(a) shows the numerically calculated dependence of the $n = 1$ Shapiro step height on the microwave current and temperature for 4096 double-stacked junctions (= 8192 JJs). The microwave bias applied to the junctions had a frequency of 16 GHz. $I_c$ and $R_n$ for the upper and lower junctions were assumed to differ by 10%. In this calculation, measured values for the temperature dependences of $I_c$ and $R_n$ were used, while the temperature dependence of $R_n$ in the temperature range of 7 to 13 K was sufficiently small for $R_n$ to be approximated by a constant value of 6 mΩ. Figure 9(b) shows the measured dependence of the $n = 1$ Shapiro step height on the microwave current and temperature for 4096 double-stacked junctions (= 8192 JJs). For both the calculations and the measurements, the maximum step heights were obtained at a temperature of about 10 K for which the product $I_cR_n$ was 33 μV; these maximum step heights were approximately equal.

Figure 10 shows the current-voltage ($I-V$) characteristics of 16 array cells in a 10-bit 1 V PJVS circuit that has double-junction stack arrays. The $I-V$s characteristics...
were measured without a microwave bias at a temperature of 10.5 K, which was obtained by cooling with a cryocooler. There are 64, 64, 128, 256, 512, 1024, 2048, 4096, and 8192 × 7 JJs in each cell. A magnetic flux trap $\delta I_c$ causes a 50% variation in $I_c$, which is much larger than the 16% variation between the upper and lower junctions $\Delta I_c$. We attempted to eliminate the magnetic flux by heating the chip above $T_c$, but it was not possible to remove all the magnetic flux. The variation in $I_c$ due to magnetic flux is currently the most critical bottleneck for improving the operating current margin.

Figure 11 shows typical current voltage characteristics of a perfect chip that has 524,288 NbN/TiN/NbN junctions irradiated by 16 GHz microwaves at 9.79 K. The inset shows that the flat step was about 1 mA, which is about five times higher than that generated by a conventional Josephson voltage standard. The total voltage was 17 V, and it was confirmed that there was no missing junction because the measured voltages generated by all 16 cells containing 32,768 JJs each agreed with the theoretical ones within the gain error of the voltmeter in a smaller voltage range [28].

4. Current Challenges

4.1 Compact Josephson Voltage Standards

Figure 12(a) shows a 10-V PJVS system that was cooled by a cryocooler rather than liquid helium. Josephson voltage standard systems are used as primary voltage standards at national metrology institutes and Zener voltage standards are used as secondary voltage standards. However, a low-cost and transportable PJVS system would be more suitable for secondary voltage standards at laboratories and factories. NbN-based JJ can reduce the volume and cost of PJVS system since they can use a more compact cryocooler due to their high critical temperature (see Fig. 12). The chip for the PJVS has a high power consumption ($\approx 100$ mW) and the binary array requires many wires for the dc bias current, resulting in a high heat flow ($\approx 300$ mW) from room temperature. An increase in the operating temperature of 1 K reduces the required cooling power by about 200 mW although it depends on the cryocooler and compressor used. Therefore, to realize a rack-mountable system it is necessary to increase the operating temperature and to reduce the output voltage.

Figure 12(b) shows a rack-mountable PJVS system that is currently being developed as a secondary standard. Except for the He gas compressor, all the components are enclosed in a chassis with dimensions 430(W) × 250(H) × 500(D) mm (19 inch 6U case). A 2-V PJVS chip rather than a 10-V PJVS chip is chosen to reduce the heat generated in the chip and an output voltage of 20 V is generated using a voltage-multiplier circuit at room temperature [29]. The intrinsic accuracy of the PJVS will be degraded by the use of semiconductor circuits, but it is sufficiently accurate as a secondary voltage standard. Since there is no secular change in the Josephson voltage standard, the period between calibrations will be reduced, which represents a significant advantage of using Josephson voltage standards as secondary voltage standards.

4.2 Ac Josephson Voltage Standards

The ac-dc transfer standard is one of the basic electrical standards by which the ac voltage and ac current are deduced from their dc counterparts for frequencies in the range 10 Hz to 1 MHz. Although dc voltage standards are established using a Josephson voltage standard, ac voltage standards are still derived from the dc voltage standard by comparing the electric power between ac and dc voltages by converting the power to heat. Therefore, direct synthesis of an ac (sine) waveform by using a high-precision D/A converter is being attempted. The Josephson arbitrary waveform synthesizer (JAWS) proposed by the NIST is one of the most promising techniques for covering a high-frequency range from kilohertz to megahertz. Benz et al. achieved
a record rms voltage of 275 mV using Nb-based JJs; they aim to eventually fabricate a 1 V system [30]. Maruyama et al. generated bipolar sinusoidal voltage waveforms at a frequency of 16 kHz with a peak-to-peak amplitude of 36.1 mV (which corresponds to an rms voltage of 12.7 mV) using 1600 NbN/TiN/NbN JJs [31]. For successful operation of JAWS with wide margins and high output voltages, many uniform JJs have to be integrated into an array. Meander arrays [16], tapered arrays [32], and self-phase-locked arrays [33] have been proposed. The next-generation ac voltage standard based on the Josephson effect is important and interesting not only for metrological studies but also from a physics perspective (e.g., redefining the Boltzmann’s constant [34]).

5. Conclusion

A 10-V PJVS using double-stacked NbN/TiN/NbN JJs was successfully demonstrated at 10 K cooled with a cryocooler. The fabrication yield for the chip containing 524,288 JJs was improved by optimizing the film growth conditions, and a design delivering the higher output voltage of 17 V also contributed to increase the number of available chips for the 10-V PJVS. The NbN-based PJVS operating at 10 K with a compact cryocooler was significantly smaller and cheaper than conventional systems, which makes it promising for use as a secondary voltage standard in laboratories and factories. We are continuing to reduce its size and cost. In addition, an arbitrary waveform synthesizer is currently being developed as a quantum ac voltage standard for metrological and industrial applications.

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References


Hirotake Yamamori was born in Toyama, Japan, in 1968. He received the B.E., M.E., and Ph.D. degrees from Nagoya University, Nagoya, Japan, in 1991, 1993, and 1996, respectively. In 1996, he joined the Electrotechnical Laboratory (ETL), presently the National Institute of Advanced Industrial Science and Technology (AIST), Tsukuba, Japan. From 2003 to 2004, he was with the National Institute of Standards and Technology (NIST), Boulder, CO, as a guest researcher.

Takahiro Yamada received the B.E., M.E., and Ph.D. degrees in quantum engineering from Nagoya University, Nagoya, Japan, in 2000, 2002, and 2006, respectively. He has been engaged in research on single-flux-quantum circuits. In 2016, he joined the National Institute of Advanced Industrial Science and Technology (AIST). His current research interests include programmable Josephson voltage standard. He is a member of the Japan Society of Applied Physics.

Hitoshi Sasaki was born in Hokkaido, Japan in 1954. He received the M.S. degree in Physics from the Hokkaido University, and Ph.D. degree in Engineering from Nagoya University. In 1979, He joined the Electrotechnical Laboratory (ETL), presently the National Institute of Advanced Industrial Science and Technology (AIST), where he has been working on precision electrical measurements. Dr. Sasaki is a member of the Japan Society of Applied Physics and the Institute of Electrical Engineers of Japan.

Satoshi Kohjiro received the B.E., M.E., and Ph.D. degrees from Kyushu University, Fukuoka, Japan, in 1984, 1986, and 1989, respectively. In 1989, he joined Electrotechnical Laboratory, presently the National Institute of Advanced Industrial Science and Technology. His specialty is superconducting mixers, oscillators, and SQUIDs. He is a member of the Japan Society of Applied Physics.