Dual-Gate ZnO Thin-Film Transistors with SiN\textsubscript{x} as Dielectric Layer

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SUMMARY We report on the fabrication of coplanar dual-gate ZnO thin-film transistors with 200-nm thickness SiN\textsubscript{x} for both top and bottom dielectrics. The ZnO film was deposited by RF magnetron sputtering on SiO\textsubscript{2}/Si substrates at 100°C. And the thickness of ZnO film is compared with 100-nm and 40-nm. This TFT has a channel width of 100-\textmu m and channel length of 5-\textmu m. The fabricated coplanar dual-gate ZnO TFTs of 40-nm-thickness exhibits a field effect mobility of about 0.29 cm\textsuperscript{2}/Vs, a subthreshold swing 420 mV/decade, an on-off ratio 2.7 \times 10\textsuperscript{7}, and a threshold voltage 0.9 V, which are greatly improved characteristics, compared with conventional bottom-gate ZnO TFTs.

key words: ZnO, TFT, dual gate, sputter

1. Introduction

ZnO-based thin film transistors (TFTs) have attracted a lot of attention because of wide band gap, transparency, and high field effect mobility, compared to that of the conventional a-Si TFTs [1]–[3]. Recent advances in ZnO-based TFTs and their application have been devoted to achieving driver or peripheral circuit components of next generation display [4]–[6]. ZnO is a material that has higher n-type conductivity unintentionally. The n-type characteristics of un-doped ZnO channel layers result from zinc interstitials or oxygen vacancies [7], [8]. Normally, there are more mobile carriers at top-side of ZnO film than bottom-side because of the increase of ZnO crystallization as-grown [9]. As for TFT structures, bottom-gate ZnO TFTs are preferred to top-gate type because higher quality of gate insulator can be made regardless of the temperature limitation by active channel formation. And turn-on voltage and hump characteristics of bottom-gate ZnO TFTs are largely dependent on oxygen concentration during ZnO sputtering in fabrication process. As ZnO TFT is deposited in low oxygen concentration relatively, large negative turn-on voltage and hump are generated by donorlike trap [10]. As we compare staggered type with coplanar type on condition of the same gate type and same oxygen concentration, coplanar type shows the depleted characteristics due to the low contact resistance. But coplanar type source/drain also presents higher on-current because of lower contact resistance than staggered type. In this study, we examined the characteristic depending on the structural change on condition that the structures of coplanar bottom gate, coplanar top gate and coplanar dual-gate in the same wafer are split in the same oxygen concentration during ZnO sputtering. Dual-gate structure on ZnO TFTs was reported by Park et al. [11]. They were made by using Al\textsubscript{2}O\textsubscript{3} as gate insulator and by using top contact of channel while our dual-gate device is manufactured using SiN\textsubscript{x} as gate insulator and using bottom contact structure. We also analyze the structural and electrical characteristics comparing bottom-gate and top-gate with dual-gate ZnO TFTs according to the channel thickness.

2. Experiment

Figure 1 is the schematic cross section and Fig. 2 is the process flow of the coplanar dual-gate ZnO TFTs with 200-nm-thick SiN\textsubscript{x} for both top and bottom dielectric. Bottom gate insulator was deposited at high temperature but top gate insulator was deposited at low temperature after ZnO deposition. The fabrication process was as follows, a 100-nm-thick Ti was deposited as a bottom gate by RF magnetron sputtering and patterned by lithography and dry etch process. Then, a 200-nm-thick SiN\textsubscript{x} was deposited as the gate insulator by conventional PE-CVD at 400°C and 100-nm-thick Ti was deposited as a channel pad by RF magnetron sputtering and patterned by lithography and dry etch process. The ZnO channel layers with 40-nm-thick and 100-nm-thick were deposited on the gate insulator and channel pad by using a RF magnetron sputtering in Ar/O\textsubscript{2} (60%/40%) at 100°C. A 50-nm-thick SiN\textsubscript{x} film was deposited on the ZnO by PE-CVD at 150°C in order to prevent the body of ZnO TFTs since the ZnO film was easily damaged by developer which were used in a photolithography process [12]. The SiN\textsubscript{x} and ZnO films were patterned by the dry etching. The dry etching gases of ZnO channel were HBr and Ar [13]. After definition of the active channel, a 150-nm-thick SiN\textsubscript{x} for the top gate insulator was deposited by PE-CVD at 150°C. Contact holes for source and drain electrodes were opened by the dry etching. And then a 100-nm-thick Ti for source/drain electrodes and a top gate was deposited by RF magnetron sputtering at room temperature and was patterned by the dry etching. The channel length and width are 5-\textmu m and 100-\textmu m, respectively. For the comparison of electrical characteristics, we also fabricated the conventional bottom-gate and top-gate ZnO TFTs on the same wafer. The ZnO and SiN\textsubscript{x}...
Fig. 1  Schematic cross-section of the dual-gate ZnO TFTs. A 200-nm-thick SiNx layer as a gate insulator is used at the both sides of ZnO channel.

Fig. 2  Conditions of film deposition for coplanar dual gate ZnO TFTs.

film thickness were measured using a spectroscopic ellipsometer and cross-sectional SEM. The structural characteristics are analyzed by XRD and the devices are electrically characterized in the air, at room temperature, and in the dark using Keithley 4200 semiconductor parameter analyzer with common bottom-gate and top-gate.

3. Results and Discussion

Figure 3 shows the capacitance-voltage (C-V) characteristics of W/L = 100-μm/100-μm. These C-V characteristics show n-channel behavior operating in accumulation mode on a positive gate bias. $C_{top}$, gate capacitance of top-gate is $2.34 \times 10^{-8}$ F/cm$^2$, $C_{bot}$ of bottom-gate value is $3.26 \times 10^{-8}$ F/cm$^2$ and $C_{dual}$ of dual-gate value is $5.87 \times 10^{-8}$ F/cm$^2$. $C_{dual}$ is equal to the summation of $C_{bot}$ and $C_{top}$. The low capacitance and poor voltage dependence of $C_{top}$ are due to depleted characteristic of top-gate insulator deposited at low temperature and high density of the intrinsic defects at top-side of ZnO [14]. And the capacitance at the depletion region for dual-gate structure is so small compared to that of bottom and top-gate structures. At C-V measurement, the ground plate positions of top and bottom-gate are contacted in the surface of ZnO while the position of dual-gate is contacted in the interface of ZnO due to structural restriction. The position difference causes to lowering the capacitance at the depletion region. Figure 4 and Fig. 5 show the transfer curves ($\log_{10}(I_D)$-$V_G$ curves) obtained from the bottom-gate, the top-gate and the dual-gate on 100-nm-thick ZnO TFTs and 40-nm-thick ZnO TFTs, respectively. The 100-nm-thick ZnO TFTs show that the turn-on voltage, $V_{ON}$ is appeared in $-20.2$ V at the bottom-gate and $-3.3$ V at the top-gate, respectively while $V_{ON}$ is about $-1.5$ V at the dual-gate. In the case of 40-nm-thick ZnO TFTs, $V_{ON}$ is appeared in $-11.3$ V at the bottom-gate and $-4.6$ V at the top-gate, respectively while $V_{ON}$ is about $-1.4$ V at the dual-gate. Here, the turn-on voltage is defined as the gate voltage corresponding to the onset of the initial sharp increase of current in a $\log_{10}(I_D)$-$V_{GS}$ curves [15]. To analyze the large difference of $V_{ON}$ of bottom gate TFTs according to the channel thick-
Fig. 5 The transfer curves (log10(\(I_D\))–\(V_G\) curves) obtained from the bottom-gate, top-gate and dual-gate for 40-nm-thick ZnO TFTs.

Fig. 6 XRD spectra and AFM RMS roughness (inset) of the ZnO films deposited at 100°C as a function of the film thickness.

Fig. 7 Schematic of a bottom-gate TFT with two parallel current paths. Here, \(I_{D,\text{Bottom}}\) is due to carriers induced by gate bias. \(I_{D,\text{Top}}\) is due to mobile carriers pre-existing at the top of channel [17].

Table 1 Device parameters of various gate types for 100-nm-thick and 40-nm-thick ZnO TFTs. Here, the field effect mobility is estimated at linear region.

<table>
<thead>
<tr>
<th>Gate types</th>
<th>100-nm-thick ZnO</th>
<th>40-nm-thick ZnO</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Bottom</td>
<td>Top</td>
</tr>
<tr>
<td>Threshold voltage [V]</td>
<td>-1.7</td>
<td>2.3</td>
</tr>
<tr>
<td>Turn-on voltage [V]</td>
<td>-20.2</td>
<td>-3.3</td>
</tr>
<tr>
<td>Saturation current [μA]</td>
<td>0.038</td>
<td>0.043</td>
</tr>
<tr>
<td>Off/On ratio</td>
<td>(1.5 \times 10^5)</td>
<td>(1.9 \times 10^5)</td>
</tr>
<tr>
<td>Subthreshold swing [V/dec]</td>
<td>0.65</td>
<td>0.56</td>
</tr>
<tr>
<td>Mobility, (\mu_{\text{FE}}) [cm²/Vs]</td>
<td>0.012</td>
<td>0.013</td>
</tr>
</tbody>
</table>

When the free carrier concentration especially at the top side becomes large enough to be normally-on, the bottom-gate TFTs can turn on in negative gate bias range causing hump. That’s why the thicker ZnO TFT is, the larger grain size is and grain boundaries as electron scattering centres could be small in the thick film. This phenomenon will be apparent as the crystallinity of the top side of the channel improves and so 100-nm-thick ZnO TFT shows more negative \(V_{\text{ON}}\).

This top current path by the mobile carriers can be controlled in the top-gate structure and so \(V_{\text{ON}}\) can be made to shift to more positive range as shown in Fig. 4 and Fig. 5. When the gate bias is applied at both side of channel as in the dual-gate type, the early \(V_{\text{ON}}\) disappears due to fully depletion of channel. This removal of parasitic current path in the dual-gate greatly contributes to the improvement of subthreshold swing (SS) as shown in Table 1 where SS in the dual-gate of 40-nm-thick ZnO is dramatically improved as 0.42 V/decade, compared with bottom-gate of 0.95 V/decade and top-gate 0.74 V/decade. The linear mobility of each gate type is also compared in Table 1 which is extracted at \(V_G-V_{\text{th}}=10\) V and \(V_{DS}=0.1\) V. The mobility is worst in top-gate structure. This is thought to be related with the depleted characteristic of top-gate insulator.
deposited at low temperature as the temperature limitation by active channel formation. The threshold voltage, \( V_{th} \) and \( On/Off \) current ratio, \( I_{On}/I_{Off} \), \( V_{th} \) is calculated at \( 10 \text{nA} \times L/W \) as constant current mode and \( I_{On} \) is estimated at \( V_{DS} = 5.1 \text{V} \) and \( V_{G} - V_{th} = 5 \text{V} \).

\( I_{Off} \) is the leakage current when the gate voltage is just below \( V_{ON} \). It can be seen that \( I_{On}/I_{Off} \) is improved 10 times better than bottom gate of \( 2.2 \times 10^6 \), as \( I_{On}/I_{Off} \) is \( 2.7 \times 10^7 \) in the dual-gate of 40-nm-thick ZnO, which is also due to the superior SS characteristics and dual current path of the dual-gate structure.

4. Conclusions

In summary, the device performance of coplanar dual-gate ZnO TFTs is dramatically improved without additional process and post treatment, compared with the bottom-gate and top-gate ZnO TFTs. This is mainly due to the improved subthreshold slope characteristics by controlling the mobile carriers at the top side which can cause hump making the parasitic current path. The mobile carriers inducing current path have the process-dependent properties which are difficult to control. Therefore, the dual-gate structure is desirable in view of fabricating ZnO TFTs with high performance and uniform characteristics.

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References


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