High Transport Si/SiGe Heterostructures for CMOS Transistors with Orientation and Strain Enhanced Mobility

Jungwoo OH†, Jeff HUANG†, Injo OK†, Se-Hoon LEE†, Paul D. KIRSCHE†, Raj JAMMY†, Nonmembers, and Hi-Deok LEE††, Member

SUMMARY We have demonstrated high mobility MOS transistors on high quality epitaxial SiGe films selectively grown on Si (100) substrates. The hole mobility enhancement afforded intrinsically by the SiGe channel (60%) is further increased by an optimized Si cap (40%) process, resulting in a combined ~100% enhancement over Si channels. Surface orientation, channel direction, and uniaxial strain technologies for SiGe channels further enhance transistor performances. On a (110) surface, the hole mobility of SiGe pMOS is greater on a (110) surface than on a (100) surface. Both electron and hole mobility on SiGe (110) surfaces are further enhanced in a ⟨110⟩ channel direction with appropriate uniaxial channel strain. We finally address low drive current issue of Ge-based nMOSFET. The poor electron transport property is primarily attributed to the intrinsically low density of state and high conductivity effective masses. Results are supported by interface trap density (Dit) and specific contact resistivity (ρc).

key words: high transport, SiGe, orientation, strain, heterostructure

1. Introduction

Strained Si channel CMOS technology has successfully extended device performance along the roadmap. Enhancements have been more significant when combined with high-k gate dielectric and metal gate technology. High mobility alternative channels continue on the high performance roadmap, where highly scaled Si channel CMOS has limitations [1]–[3]. SiGe and other high mobility channels potentially provide high injection velocity to achieve projected high performance metrics.

Ge-based channel pMOSFETs fabricated on high quality epitaxial films selectively grown on Si (100) substrates exhibit enhanced hole mobility. With a Si cap processed on Ge channels, high-k gate dielectrics exhibited low C-V hysteresis, interface trap density, and gate leakage current, which are comparable to gate stack on Si channels [4]. The mobility enhancement afforded intrinsically by the Ge channel is further increased by a Si cap process [5].

To enhance mobility in nMOS and pMOS, dual channel materials (Ge for pMOS or III-V for nMOS) or hybrid Si surface orientation approaches have been demonstrated [6]; however, they might increase integration complexity. For a practical approach, the integration of high mobility CMOS transistors on a single channel is preferable. While the mobility enhancement for Ge pMOSFETs has been well reported, few studies have been able to improve Ge nMOSFET mobility after optimizing the gate stack and parasitic resistance. Recently, enhanced electron mobility of Ge nMOSFETs was demonstrated in long channel transistors [7]–[9].

2. Device Fabrication

High quality epitaxial SiGe channels are selectively grown on shallow trench isolation-formed Si substrates. A Si cap layer is deposited to improve the interface characteristics and off-state current as shown in earlier report [10]. The Si cap process mitigates the low potential barrier issues of SiGe channels, which are major causes of the high off-state current of small bandgap energy SiGe pMOSFETs. ALD Hf-based gate oxide is deposited followed by the metal gate. The TEM image (Fig. 1) shows a high-k gate dielectric and metal gate fabricated on a SiGe-on-Si substrate.

3. Results and Discussion

Figure 2 compares C-V curves of SiGe MOS capacitors (25% and 40% Ge). EOT of 13.6 Å and 14.0 Å were extracted using CVC model from 25% and 40% Ge capacitors, respectively. The physical thickness of HfSiO2 is 40 Å. Minimal C-V hysteresis at 1 MHz was measured to
Fig. 2 C-V of SiGe MOS capacitors with low EOT and minimal hysteresis. Gate leakage current density ($J_g$) of HfSiO$_2$ dielectric on SiGe channel pMOSFETs.

Fig. 3 Gm enhancement afforded intrinsically by the SiGe channel (Ge=25%) is further increased by an optimized Si cap, resulting in a combined ~100% enhancement over Si channels.

Mobility enhancement was supported in the transconductance (Gm) results in Fig. 3. SiGe channels (Ge=25%) without a Si cap (EOT=14.1) exhibited ~60% Gm enhancement over the Si channels (EOT=13.2). After applying the Si cap process (deleted) on SiGe channel (EOT=13.4), Gm was further enhanced by ~40%. Therefore, a ~100% enhancement was achieved by the combined SiGe channel and Si cap processing.

For further hole mobility enhancement, we have introduced a SiGe (110) surface orientation, varying channel direction, and uniaxial strain to boost the performance of pMOS and nMOS simultaneously [11],[12]. Fig. 4 shows the available channel directions: (110), (100) for a (100) surface; and (110), (111), (100) for a (110) surface. It also shows MOSFETs with varying channel directions: 0° (conventional), 45°, 90°, and 135°.

For the pMOS on (100) surface (Fig. 5), the ⟨100⟩ direction enhances Gm in Si (8%) and in SiGe (18%) as compared to the ⟨110⟩ direction. This enhancement factor becomes more significant for SiGe pMOS on (110) surfaces where the ⟨110⟩ direction enhances Gm 60% more than ⟨100⟩ direction.

Finally, we address low drive current issue of Ge-based nMOSFET. The poor electron transport property is primarily attributed to high interface trap density near the conduction band edge and high series S/D resistance. In this work, we propose the intrinsically low density of state and high conductivity effective masses [13]. Results are supported by interface trap density (Dit) and specific contact resistivity ($\rho_c$). Figure 6. compares transconductance (Gm) of Si and Ge channels. For Ge pMOSFETs, $I_d$ increases as Ge % increases in the channel due to enhanced hole mobility as previously reported. For Ge nMOSFETs, however, $I_d$ decreases dramatically as Ge % increases.

It is likely that most electrons populate the L valleys for a (001) [110] Ge nMOSFET channel direction (Fig. 7). Effective masses projected on the (100) plane are strongly affected by L valleys in a way that is consistent with the Schrodinger equation. Effective masses of electrons, which populate L valleys are large for conductivity and small for the density of states in conventional (100) [110] channel directions, resulting in low electron mobility and carrier concentration in Ge-based nMOSFETs.

The large conductivity effective mass and low density of state effective mass of L valleys compromise carrier mobility and carrier concentration and, therefore, degrades transport characteristics of (001) [110] Ge nMOSFETs. The small electron population in $\Gamma$ valleys with very small ef-
Fig. 4  Channel directions and rotated (0° − 135°) MOSFETs; (110) and (100) for a (100) surface and (110), (111), and (100) for a (110) surface. 2D sub-band energy diagrams: (b) SiGe (100) and (c) SiGe (110) surface.

Fig. 5  (100) enhances pMOS Gm in both Si (8%) and SiGe (18%) than (110) on (100) surface. More significant gain (60%) is achieved for SiGe pMOS on (110) (110).

Effective mass 0.044 \( m_0 \) that contributes to bulk Ge electron mobility may account for the low inversion electron mobility of Ge nMOSFETs.

The relative performance of Si and Ge MOSFETs is in good agreement with total on-resistance (\( R_{\text{total}} \)) vs. gate length (\( L_g \)) results. For nMOSFETs, \( R_{\text{total}} \) of the Ge channel is higher than the Si channel, resulting in low drain current in Ge nMOSFETs. For pMOSFETs, \( R_{\text{total}} \) of the Ge channel is lower than the Si channel and enhanced transport characteristics were obtained.

4. Conclusions

Optimized Si caps reduced interface trap density and showed minimal C-V hysteresis. Si cap processing effectively suppressed the off-state current of SiGe pMOSFETs by providing better gate control over the channel, while enhancing hole mobility by 40% in the SiGe channel, which resulted in a ~100% mobility enhancement over Si channels. Carrier mobility is enhanced on a SiGe (110) surface orientation with additive gains in the (110) channel direction. Further mobility enhancement is achieved with uniaxial strain, suggesting sustainable process-induced strain technology as a SiGe (110) CMOS performance booster. Large conductivity and small density of state effective
masses of (001) [110] Ge sub-valleys cause low mobility and carrier concentration, resulting in low on-state current of Ge-based nMOSFETs.

References


Jungwoo Oh  holds a doctorate in materials science and engineering from the University of Texas at Austin. He earned a master’s degree in materials science and engineering from POSTECH and a bachelor’s degree from Yonsei University in Korea. He works as a Member Technical Staff within SEMATECH’s Materials & Emerging Technology Division. Dr. Oh is conducting nanoscale advanced CMOS devices using a variety of semiconductor materials and processing. Dr. Oh’s research includes system on chip integration of III-V-on-Si photonics and electronics for display, telecommunication, and energy devices.

Jeff Huang  was born in Taiwan in 1975. He received the M.S. and Ph.D. degrees in the electronics engineering from National Chiao Tung University, Taiwan in 2001 and 2006, respectively. He joined SEMATECH, Texas, USA in 2006, where he worked on the development of Front End CMOS process. He is an author or coauthor of more than 60 publications.

Injo Ok  received the B.S. and M.S. degrees in Electrical Engineering from Changwon National University, Changwon, Korea in 2000 and 2002, respectively and the Ph.D. degree in Electrical and Computer Engineering at the University of Texas, Austin. In April 2008, he joined Sematech at Albany, Albany, NY, where he works on fabrication and characterization of III-V and SiGe FinFET transistors for 22-nm node and beyond. He has authored or coauthored more than 47 technical papers.

Se-Hoon Lee  (S’06) was born in Seoul, Korea. He received the B.S. degree in electrical engineering from Seoul National University, Seoul, Korea, in 2004 and the M.S. degree in electrical and computer engineering from The University of Texas at Austin, in 2007, where he is currently working toward the Ph.D. degree. From 2006 to 2010, he was a Device Intern and a visiting Research Student with SEMATECH’s Emerging Technology Division (SE-MATECH) Inc., Austin. His research interest includes heteroepitaxy of group IV semiconductor materials by chemical vapor deposition, fabrication of scaled high-mobility channel MOSFETs, and electrical characterizations on carrier transport properties and reliability of MOSFETs.
Paul D. Kirsch received a B.S. (1995) in chemical engineering from the University of Wisconsin-Madison and Ph.D. (2001) in chemical engineering from the University of Texas at Austin. He has been with IBM Systems and Technology Group since 2001. His work has focused on gate stack development. He has authored and co-authored more than 25 journal and conference papers in the various semiconductor research areas including high-k dielectric surface and interface chemistry, atomic layer deposition and high-k dielectric/metal gate devices.

Rajarao “Raj” Jammy graduated with a doctoral degree in Electrical Engineering from Northwestern University in November 1996. He then joined IBM’s Semiconductor Research and Development Center in East Fishkill, NY, where he worked on development of ultra-thin dielectrics, advanced doping techniques and other front end of line technologies for deep trench DRAMs. In January 2001 he was appointed as Manager of the Thermal Processes, and Surface Preparation group with additional responsibilities in CMP, Thin Films and Metallization in the DRAM development organization. He moved to IBM T. J. Watson Research Center in Yorktown Heights, NY in June 2002 to manage IBM’s efforts on high k gate dielectrics and metal gates. Between June 2005 and June 2008 he was an IBM assignee to SEMATECH as the Director of the Front End Processes Division in Austin, TX. In June 2008 he joined SEMATECH staff after the completion of his assignment from IBM. As SEMATECH staff his responsibilities were expanded, and he currently serves as the Vice President of Emerging Technologies. He holds more than 50 patents and is an author/co-author of over 125 publications/presentations.

Hi-Deok Lee received the B.S., M.S., and Ph.D. degrees in electrical engineering from the Korea Advanced Institute of Science and Technology, Daejeon, Korea, in 1990, 1992, and 1996, respectively. In 1996, he joined the LG Semicon Company, Ltd. (currently Hynix Semiconductor Ltd.), Chongju, Choongbuk, Korea, where he has been involved in the development of 0.35-, 0.25-, and 0.18-μm CMOS technologies, respectively. He was also responsible for the development of 0.15- and 0.13-μm CMOS technologies. Since 2001, he has been with Chungnam National University, Daejeon, Korea, and now is a Professor with the Department of Electronics Engineering. From 2006 to 2008, he was with the University of Texas, Austin, and SEMATECH, Austin, as a Visiting Scholar. His research interests are in the areas of nanoscale CMOS technology and analog MOSFET technology and their reliability physics, analysis and modeling of low frequency noise, silicide/germanide technology, and Test Element Group design. His research interests also include RF CMOS device modeling, circuit design, crosstalk, and time delay modeling of interconnection lines. Dr. Lee is a member of the Institute of Electronics Engineers of Korea.