Phase Compensation Techniques for Low-Power Operational Amplifiers

SUMMARY An operational amplifier is one of the key functional blocks and is widely used in analog and mixed-signal circuits. For low-power consumption, many techniques such as class AB and slew-rate enhancement have been proposed. Although phase compensation is related to power consumption, it has not been clearly discussed from the viewpoint of the power consumption. In this paper, the conventional and the improved Miller compensations and the phase compensation by introducing a new zero are discussed for low-power operational amplifiers.

key words: low-power, operational amplifier (opamp), phase-compensation

1. Introduction

The operational amplifier (opamp) is the most basic circuit in the analog circuit, and it has been widely used in many applications. For example, in cellular phones as shown in Fig. 1, the opamp is used in an audio, a microphone, a liquid crystal display (LCD) and a transceiver IC. In the direct conversion transceiver shown in Fig. 2, the opamp is used in the analog baseband circuits such as low-pass filter (LPF), variable gain amplifier (VGA) and analog/digital converter (ADC) [1]–[4]. In the LCD driver circuit shown in Fig. 3, the opamps are used for the buffer amplifiers that drive the signal lines on the LCD panel [5], [6]. Several hundred opamps are integrated in a single chip, the power consumption of opamps becomes dominant. In battery driven equipment such as a cellular phone, low-power consumption is required for expanding talk time and standby time. Much research has been done to reduce power consumption of opamps.

Class B [7], [8], class AB [9]–[14], push-pull [15], [16], dynamic bias (DB) [17], [18], dynamic amp (DA) [19], and slew-rate enhancement (SRE) [5], [20]–[22] have been reported for reducing the power consumption of opamps.

In the class B output stage, when there is no input signal, the current of the output stage becomes zero. Only when the input signal amplitude becomes larger than the predetermined value, the current of output stage increases according to the input signal amplitude. Since the power consumption depends on the input signal amplitude, the power consumption of the opamp can be reduced. However, crossover distortion, which occurs for small input signal amplitudes, should be taken into account to achieve good linearity. Class AB output stage flows small bias current even when there is no or small input signal. This improves the linearity of the opamp. Class B and class AB are used in order to reduce the power consumption in LPF, VGA and the buffer that operate at continuous time.

DB and DA are used in the switched-capacitor (SC) circuits and sample-hold (SH) circuits that operate at discrete time. In these techniques, the bias current is applied to the opamp at clock rising or falling edges.

SRE is the technique for reducing the power consumption, which is also suitable for discrete-time applications such as SC circuits and LCD driver circuits. SRE senses the difference between the plus and the minus input voltages, and increases the bias current of the opamp when the difference is larger than the predetermined level.

The research on reducing the power consumption by improving the drive capability of the opamp has been dis-
discussed in many papers. On the other hand, the phase compensation has not been clearly discussed from the viewpoint of the reduction of the power consumption, although the improvement of the compensation and the reduction of the compensation capacitance have been reported in many papers [23]–[25]. For example, in the LCD driver circuits, the settling time is important and is affected by the slew rate, which the compensation capacitance and the bias current affect. So, the phase compensation is a crucial issue in the context of efforts to reduce the power consumption of the opamp. In the wideband wireless applications such as LTE [26] and WiMAX [27], the phase compensation of the opamp is also crucial to satisfy both wide bandwidth and low-power consumption.

In this paper, the phase compensation techniques are discussed from the viewpoint of reducing the power consumption.

2. Conventional and Improved Miller Compensation Techniques

The well-known phase compensation technique is the Miller compensation shown in Fig. 4. The small signal equivalent circuit of the Miller compensation is shown in Fig. 5. The transfer function, \( H_{mil}(s) \), of the Miller compensation is obtained as follows;

\[
H_{mil}(s) \approx A_{mil} \frac{1 - s/z_{mil}}{(1 - s/p_{1mil})(1 - s/p_{2mil})}
\]

\[\begin{align*}
A_{mil} &= \frac{g_{m1} g_{m2}}{g_{o1} g_{o2}} \\
p_{1mil} &= \frac{g_{o2} g_{o1}}{g_{m2} C_C} \\
p_{2mil} &= \frac{g_{m2} C_L}{C_L C_1 + C_L C_C + C_C C_1} \\
z_{mil} &= \frac{g_{m2}}{C_C}
\end{align*}
\]

where \( A_{mil} \) is the total DC gain, \( p_{1mil} \) and \( p_{2mil} \) are the first and the second poles, \( z_{mil} \) is the zero, \( g_{m1} \) and \( g_{m2} \) are transconductances of the input and the output stages, \( g_{o1} \) and \( g_{o2} \) are the output conductance of the input and output stages, \( C_1 \) is the parasitic capacitance at the output of the input stage, \( C_C \) is the phase compensation capacitor, \( C_L \) is the load capacitance at the output, and \( I_1 \) and \( I_2 \) are the bias currents of the input and the output stages. Assuming that the current drive-capability of the output stage is sufficiently high, the slew rate, \( SR_{mil} \), of the opamp is limited as follows;

\[
SR_{mil} = \frac{I_1}{C_C}
\]

In order to achieve the stability of the opamp, it is necessary to guarantee the phase margin. For larger \( C_L \), larger \( C_C \) and/or larger \( g_{m2} \) are required to achieve the same phase margin. Larger \( I_1 \) is also necessary for keeping the same slew rate for larger \( C_C \).

The improved Miller compensation shown in Fig. 6 has been reported [28], where the second pole can be moved to a higher frequency without increasing \( g_{m2} \). The improved Miller compensation is formed by adding the common-gate current buffer to the conventional Miller compensation. The phase compensation capacitor is connected between the output and the source node of the common-gate buffer. The small signal equivalent circuit of the improved Miller compensation is shown in Fig. 7. The transfer function, \( H_{imc}(s) \),

of the improved Miller compensation is obtained as follows;

\[ H_{\text{imc}}(s) \approx \frac{A_{\text{imc}}}{1 - s/p_{1\text{imc}}}(1 - s/p_{2\text{imc}}) \]  

(7)

\[ A_{\text{imc}} = \frac{g_{m1} g_{m2}}{g_{o1} g_{o2}} \]  

(8)

\[ p_{1\text{imc}} = -\frac{g_{o2}}{g_{m2}} C_C \]  

(9)

\[ p_{2\text{imc}} = -\frac{g_{m2} C_C}{C_1(C_C + C_L)} \]  

(10)

where \( A_{\text{imc}} \) is the total DC gain, and \( p_{1\text{imc}} \) and \( p_{2\text{imc}} \) are the first and the second poles. The improved Miller compensation has two advantages over the conventional Miller compensation. One is no low-frequency zero in right-half plane, the other is a higher-frequency second pole.

In the conventional Miller compensation, there is a frequency at which the current flowing through \( C_C \) cancels the drain current of M5, i.e., a zero exists. This zero locates in the right-half-plane, and it degrades phase margin. In the improved Miller compensation, the feedforward current from the drain of M6 to the source of M6 is almost zero. This makes the zero move to very high frequency and not degrade the phase margin.

Comparing Eqs. (3) and (9), the first poles of the Miller compensation and the improved Miller compensation are almost equal. But, the second pole of the improved Miller compensation is higher than that of the conventional Miller compensation by the following ratio:

\[ \frac{p_{2\text{imc}}}{p_{2\text{mil}}} = \frac{C_L C_1 + C_L C_C + C_C C_1}{C_1(C_C + C_L)} \]  

(11)

Assuming that the opamp drives the large capacitive load, for the case of \( C_1, C_C \ll C_L \), (11) can be approximated;

\[ \frac{p_{2\text{imc}}}{p_{2\text{mil}}} \approx \frac{C_C}{C_1} \]  

(12)

\( C_1 \) is usually smaller than \( C_C \). The required \( C_C \) can be reduced to obtain the same phase margin as the conventional Miller compensation. With smaller phase compensation capacitance, it is possible to reduce the current of the input stage required for the specified slew rate (6).

The improved Miller compensation shown in Fig. 6 requires an additional bias current. In order to apply the improved Miller compensation without increasing the current consumption, the phase compensation techniques using a self-cascode circuit have been proposed, where the self-cascode is applied to the transistor forming the active load at the input stage (Fig. 8, [5]) or the transistor forming the input differential pair (Fig. 9, [29]). In Fig. 8, the phase compensation capacitor is connected between the drain of M7 and the source of M6 is almost zero. This makes the zero move to very high frequency and not degrade the phase margin.

Comparing Eqs. (3) and (9), the first poles of the Miller compensation and the improved Miller compensation are almost equal. But, the second pole of the improved Miller compensation is higher than that of the conventional Miller compensation by the following ratio:

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In the phase compensation techniques using self-cascode circuit mentioned above, unless the multi $V_{th}$ process is used, M5 and M6 in Fig. 8 and M1 and M2 in Fig. 9 operate in a linear region. So, all feedback current from the phase compensation capacitor $C_C$ does not flow into the common-gate current buffer; some feedback current flows into the transistor operating in a linear region. This should be taken into account in determining the phase compensation capacitor $C_C$ [5].

3. Phase Compensation Techniques with No On-Chip Capacitor

Even with the improved Miller compensation technique, a large Miller capacitance and/or a high $g_m$ of the output stage is necessary to drive a large capacitive load. These two approaches still increase the power consumption of the opamp. Phase compensation techniques with no on-chip capacitor have been reported. The techniques introduce a new zero for phase compensation [30], [31].

3.1 Phase Compensation Using Capacitive Load

The introduction of zero can be realized by using the capacitive load [30]. The circuit configuration of this technique is shown in Fig. 10. A resistor is connected between the output of the opamp and the large capacitive load, and the transfer function from $V_{in}$ to $V_{out1}$, $H_{ac}(s)$, of Fig. 10 is obtained as follows;

$$H_{ac}(s) = \frac{1 - s/z_{ac1}}{A_{ac1}}$$  \hspace{1cm} (13)

$$A_{ac1} = \frac{g_{m1}g_{m2}}{g_{o1}g_{o2}}$$  \hspace{1cm} (14)

$$P_{1ac1} = \frac{g_{o1}}{C_L}$$  \hspace{1cm} (15)

$$P_{2ac1} = \frac{g_{o2}}{C_1}$$  \hspace{1cm} (16)

$$z_{ac1} = -\frac{1}{R_ZC_L}$$  \hspace{1cm} (17)

This transfer function, $H_{ac}(s)$, has two poles and one zero. Because this zero locates in the left-half-plane, this zero is utilized in the phase compensation. As shown in Fig. 11, the resistance $R_Z$ is designed to insert the zero between the second pole and the unity gain frequency. Since the frequency response around the unity gain frequency becomes close to the one pole characteristic, it is possible to obtain the phase margin. Even when the load capacitance is large, it is not necessary to increase the bias current from the viewpoint of phase compensation. This phase compensation technique with the class AB output stage is suitable for the buffer amplifier for the LCD driver to reduce the power consumption.

Note that the drive capability of the opamp is limited in $R_Z$ and $C_L$. As shown in Fig. 10, the transfer function of the opamp is obtained with $V_{out1}$ as the output node. However, the actual output node is $V_{out2}$ where the load capacitance $C_L$ is connected. $V_{out2}$ becomes dull owing to LPF formed by $R_Z$ and $C_L$. The high-speed phase compensation using capacitive load to alleviate the degradation due to this LPF has been proposed [31]. As shown in Fig. 12, the output stage of this circuit is formed with two parallel stages ($g_{m2}$ and $g_{m3}$ in Fig. 12). One output stage $g_{m2}$ is the same configuration as Fig. 10. Another output stage $g_{m3}$ is connected to the load capacitance $C_L$ directly to realize a high slew rate. The transfer function, $H_{hsu}$, of Fig. 12 is obtained as follows;

$$H_{hsu}(s) = \frac{A_{hsu}}{(1 - s/z_{hsu})}$$  \hspace{1cm} (18)

$$A_{hsu} = \frac{g_{m1}g_{m2} + g_{m3}}{g_{o1}g_{o2} + g_{o3}}$$  \hspace{1cm} (19)

$$P_{1hsu} = -\frac{g_{o2} + g_{o3}}{C_L}$$  \hspace{1cm} (20)

$$P_{2hsu} = -\frac{g_{o1}}{C_1}$$  \hspace{1cm} (21)

$$z_{hsu} = -\frac{g_{m2} + g_{m3}}{R_ZC_L}$$  \hspace{1cm} (22)

The zero indicated in (22) shifts to a higher frequency than

![Fig. 10](image1)

**Fig. 10** Phase compensation using capacitive load.

![Fig. 11](image2)

**Fig. 11** Example of open-loop frequency characteristics of phase compensation using capacitive load.

![Fig. 12](image3)

**Fig. 12** High-speed phase compensation using capacitive load.
that indicated in (17) by the ratio of the transconductance of two output stages \((g_{m2} + g_{m3})/g_{m2}\). This shift should be taken into account in design. To insert the zero in the same frequency as the zero (17) in Fig. 10, it is necessary to increase \(R_Z\) by this ratio \((g_{m2} + g_{m3})/g_{m2}\). Because the techniques in Fig. 10 and Fig. 12 do not use the Miller capacitance, these techniques can reduce the power consumption of the input stage even when the load capacitance is large.

3.2 No Capacitor Feedforward Phase Compensation

There is the phase compensation technique suitable for wideband width that utilizes the zero without shifting the first and the second poles of the opamp to higher frequencies. This phase compensation technique needs two circuit blocks. One is the two-stage amplifiers and another is the single-stage amplifier as shown in Fig. 13. The frequency responses of these two amplifier are combined as shown in Fig. 14. At high frequencies, the frequency response of the single-stage amplifier is dominant and vice versa at low frequencies. This means that a zero is introduced in the combined frequency response [32], [33]. The transfer function, \(H_{nc}\), of this circuit is obtained as follows;

\[
H_{nc} \approx A_{nc} \frac{(1 - s/z_{nc})}{(1 - s/p_{1nc})(1 - s/p_{2nc})} \quad (23)
\]

\[
A_{nc} \approx \frac{g_{m1} g_{m2}}{g_{o1} (g_{o2} + g_{o3})} \quad (24)
\]

\[
p_{1nc} = -\frac{g_{o1}}{C_{1}} \quad (25)
\]

\[
p_{2nc} = -\frac{g_{o2} + g_{o3}}{C_{L}} \quad (26)
\]

This transfer function, \(H_{nc}\), has two poles and one zero. When the unity gain frequencies of the two-stage and single-stage amplifiers are the same, the introduced zero locates at the unity gain frequency, and the phase margin is about 45°.

3.3 Comparison between Miller Compensation and No Capacitor Feedforward Phase Compensation

When the opamp is used in the LPF, the power consumption of the opamp with the Miller compensation is compared with that of the opamp with no capacitor feedforward phase compensation. The opamp is used as an integrator in the filter as shown in Fig. 15. In this configuration, the load of \(G_m1\) is the resistance, \(R_Z2\). \(R_Z2\) is connected between the output of \(G_m1\) and the virtual short node of \(G_m2\). \(C_1\) and \(R_Z1\) form the integrator with \(G_m1\). A sufficient gain of the opamp around the unity gain frequency of the integrator, \(\omega_{u-int}\), is required. Here, \(A_{req}\) denotes the required gain at \(\omega_{u-int}\). Generally, the gain of the opamp at \(\omega_{u-int}\) should be sufficiently large, for example, 40 dB.

In the Miller compensation, the bandwidth of the opamp after compensation should be expanded as shown in Fig. 16, when the gain at \(\omega_{u-int}\) after compensation is lower than \(A_{req}\). In the no capacitor feedforward phase compensation, although it is unnecessary to expand the bandwidth of the two-stage amplifier, the single-stage amplifier is added as shown in Fig. 13. Therefore, a current increase for expanding the bandwidth in the Miller compensation and a current increase for adding single-stage amplifier are compared. For simple calculation, the currents of the input stage and the output stage of the two-stage amplifier and the single-stage amplifier are increased to keep the current density of the transistors constant. When the current of the
transistor increases N times, the channel width of the transistor is increased N times. Then \( g_m \) and \( g_o \) also increase N times.

Figure 17 shows a simple two-stage amplifier. \( g_{m1} \) is transconductance of the input stage, \( g_{m2} \) is transconductance of the output stage, \( g_{o1} \) is the output resistance of the input stage, \( g_z \) denotes the load resistance as a conductance representation, \( C_1 \) is the input capacitance of the output stage, and \( C_2 \) is the output capacitance. The current consumption of the Miller compensation and no capacitor feedforward phase compensation are compared in the following two conditions: (a) \( \omega_{u-int} \) is low and (b) \( \omega_{u-int} \) is high.

In the first condition, \( \omega_{u-int} \) is sufficiently low and the gain of the opamp at \( \omega_{u-int} \) after the Miller compensation is greater than \( A_{req} \) as shown in Fig. 18. In this condition, no current increase is required when the Miller compensation is applied. On the contrary, when the no capacitor feedforward phase compensation is applied, the current increase of the additional single-stage amplifier is required. Therefore, when \( \omega_{u-int} \) is sufficiently low, the Miller compensation is better than the no capacitor feedforward phase compensation.

In the second condition, \( \omega_{u-int} \) is high and the gain of the opamp at \( \omega_{u-int} \) after the Miller compensation is lower than \( A_{req} \) as shown in Fig. 19. In this condition, it is necessary to expand the bandwidth of the uncompensated opamp by increasing the transconductances of the input and the output stages with the current increase. The required unity gain frequency, \( \omega_{u-req} \), is obtained as follows:

\[
\omega_{u-req} = A_{req} \omega_{u-int}
\]  

where \( \omega_{u-int} \) and \( \omega_{u-req} \) are the first and the second poles of the uncompensated opamp. Here the current density of the transistors are assumed to be kept constant when increasing their transconductances. That is, when \( g_{m1} \) and \( g_{m2} \) are increased by \( L \) times, the currents and channel widths of the transistors in the input and the output stages are increased by \( L \) times. Then, \( C_1 \) also becomes \( L \) times larger. Therefore, when increasing \( \omega_{u-unc} \) by \( N \) times, the currents of the input and the output stages should be increased by \( N^2 \) times, for example.

When the no capacitor feedforward phase compensation is applied to this opamp in this condition, the current consumption of the additional single-stage amplifier is analyzed. The unity gain frequency of the single-stage amplifier, \( \omega_{u3} \), is obtained as follows:

\[
\omega_{u3} = \frac{g_{m3}}{C_2}
\]  

The \( \omega_{u3} \) is designed to be the same or higher than \( \omega_{u-unc} \). The smallest \( g_{m3} \) is obtained when \( \omega_{u3} \) is equal to \( \omega_{u-unc} \) as shown in Fig. 20. Then the smallest \( g_{m3} \) is obtained as follows:

\[
g_{m3} = \sqrt{\frac{C_2}{C_1 g_{m1} g_{m2}}}
\]  

In order to express the current required for \( g_{m3} \) by using the current for \( g_{m2} \). Equation (34) is divided by \( g_{m2} \).

\[
\frac{g_{m3}}{g_{m2}} = \sqrt{\frac{C_2 g_{m1}}{C_1 g_{m2}}}
\]
\[ I = \frac{\sqrt{A_1 p_1}}{A_2 p_2} \tag{36} \]

where \( A_1 \) and \( A_2 \) are the gains of the input and the output stages, respectively. Therefore, the required current of \( g_{m3} \) is calculated by using \( A_1, A_2, p_1 \) and \( p_2 \).

In the Miller compensation, as \( \omega_{u-int} \) is higher frequency, the required additional current becomes higher. In the no capacitor feedforward compensation, the required additional current does not depend on \( \omega_{u-int} \), and is constant as long as the gain at \( \omega_{u-int} \) in uncompensated condition is greater than \( A_{req} \). Therefore, when \( \omega_{u-int} \) is sufficiently high, the no capacitor feedforward phase compensation is better than the Miller compensation.

4. Design Examples

The techniques of the phase compensation mentioned above that reduce the power consumption of the opamp are applied to the buffer amplifier for the LCD driver [34] and the opamp for the wideband LPF [35].

4.1 A Low-Power Opamp for LCD Driver

For the LCDs used in mobile terminals, low power consumption is the most important requirement. According to Ref. [30], current consumption of a few \( \mu A \) or less is required for the individual buffer amplifiers in the column driver. Recently, high resolution is required and the number of the signal lines on the panel has increased. Since it is physically difficult in the column driver to provide the same number of pads as the corresponding signal lines, one buffer amplifier drives plural signal lines as shown in Fig. 21, which is called time-sharing drive. In this architecture, the settling time allowed to drive one signal line becomes shorter than that in the non-time-sharing drive architecture. According to Ref. [30], the settling time is below 30\( \mu \)sec. When the time-sharing drive architecture is employed, the settling time becomes 4\( \mu \)sec in the case that the individual buffer amplifiers drive 6 signal lines, considering the line-switching time. When 9 signal lines are driven by one buffer amplifier, the settling time becomes 2\( \mu \)sec.

Since a signal line on the LCD panel is capacitive, the phase compensation using capacitive load is applied. But, while switching the signal lines in the time-sharing architecture, no load is connected to the amplifier. In no load condition, it is impossible to utilize the technique of phase compensation using capacitive load. Therefore, additional phase compensation such as the Miller compensation is necessary to guarantee the stability of the amplifier in no load condition. However, when the Miller compensation capacitor is simply applied, a slew rate is limited by the Miller compensation capacitor and the bias current of the input stage. Here, the phase compensation technique suitable for the voltage follower configuration shown in Fig. 9 is applied.

In order to satisfy the requirements for the power consumption of a few \( \mu A \) or less, it is also important to reduce the power consumption with the improvement of drive capability of the output stage. Therefore, class AB output stage that utilizes the floating class AB control is used in the buffer amplifier [12]. The buffer amplifier for the LCD driver with the above-mentioned techniques is shown in Fig. 22 [34]. In the LCD driver, because the buffer amplifier drives the liquid crystal cell between the ground and the power supply voltage, a rail-to-rail input/output is required for the buffer amplifier. Therefore, the rail-to-rail input stage is formed by the configuration such that output currents from NMOS and PMOS differential pairs are added at the floating class AB control block.

The simulated frequency responses when the opamp drives the large capacitive load and no load are shown in Fig. 23. When the opamp drives the large capacitive load, the zero is inserted at about 1 MHz. When the opamp drives no load, the frequency response shows the normal Miller compensation response. Finally, the phase margin is 57° for
driving large capacitive load, and $37^\circ$ for driving no load. Because two phase compensation techniques are utilized in parallel, sufficient phase margin is achieved when the opamp drives the large capacitive load and no load.

The opamp shown in Fig. 22 is fabricated with 0.13 μm CMOS process technology. A layout image is shown in Fig. 24. The layout area of the opamp is 100 μm × 45 μm without pads area. The supply voltage is 5 V, the current consumption is 2 μA. A load resistance is 10 kΩ, and a load capacitance including probe capacitance is 24 pF. When an input signal changes from 0.5 V to 4.5 V and from 4.5 V to 0.5 V, the input/output voltages are shown as in Fig. 25. The settling time within ± 10 mV is 1.95 μsec at rising edge and 1.29 μsec at falling edge. The measurement summary of the opamp for LCD driver is shown in Table 1. Because both settling times are below 2 μsec, the opamp can be employed in the 9 signal lines selecting time-sharing drive architecture. Since one opamp can drive nine signal lines, the corresponding current consumption per signal line is 0.22 μA.

<table>
<thead>
<tr>
<th>Table 1 Measurement summary of LCD driver amplifier.</th>
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<tr>
<td>Supply voltage</td>
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<td>Quiescent current consumption</td>
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<td>Settling time at rising edge</td>
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<td>Settling time at falling edge</td>
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<td>Current consumption /line</td>
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4.2 An Opamp for Low Supply-Voltage Wideband Filter

In the wideband wireless applications such as LTE [26] and WiMAX [27], the bandwidth of analog baseband circuit is 10 MHz. In the WLAN 802.11n [36], the bandwidth of analog baseband circuit is 20 MHz. The gate length of transistor has been decreased by improving the CMOS process technology. In finer process technologies, the maximum power supply voltage becomes lower. This deteriorates the distortion of the signal. The balanced OTA shown in Fig. 26 is suitable for low power-supply voltage, where the transconductor of the balanced OTA shown in Fig. 27 can be composed only of common-source amplifiers. In the balanced OTA, the transistor for the tail current source of differential pair shown in Fig. 4 is removed so that the minimum input voltage of the balanced OTA can be lower than the minimum input voltage of the conventional differential pair.

The Miller compensation capacitor has been applied to the conventional balanced OTA shown in Fig. 27 for the phase compensation of two-stage amplifier [4]. No capacitor feedforward compensation is applied to the balanced OTA as shown in Fig. 28 to expand the bandwidth of the balanced OTA [35]. No capacitor feedforward compensation balanced OTA is realized by the parallel connection.
of two-stage balanced OTA and single-stage balanced OTA. Because the GBW for common-mode signal of the balanced OTA is the same as the GBW for differential-mode signal of the balanced OTA, it is necessary to apply the phase compensation for the common-mode signal. Because the single-stage amplifier is also composed of the balanced OTA, no capacitor feedforward compensation can be applied to the common-mode signal by connecting the common-mode feedback of the two-stage amplifier and the common-mode feedback of the single-stage amplifier. The frequency response is shown in Fig. 29. The zero is introduced at about 600 MHz. For lower frequencies than 600 MHz, the frequency response of the two-stage amplifier is dominant. For higher frequencies than 600 MHz, the frequency response of the single-stage amplifier is dominant. The phase margin of this opamp is about 25° to minimize the current increase by the single-stage amplifier. This opamp has 47 dB gain at 10 MHz.

The 5th-order Chebyshev LPF for WLAN 802.11a/b/g shown in Fig. 30 by using no capacitor feedforward compensation balanced opamp is designed with the leap-frog configuration. The frequency response of this LPF is shown in Fig. 31. The frequency response of the measurement is almost equal to that of the simulation. Figure 32 shows IP1 dB of this LPF. The output voltage swing of 700 mVpp is obtained.

The analog baseband receiver circuit that operates at 0.9 V power supply can be composed by combining with Delta Sigma modulator of [4]. Table 2 shows the measurement summary.

### 5. Conclusions

In this paper, the phase compensation is discussed from the viewpoint of the power consumption. Depending on the applications, it should be carefully considered which
phase compensation technique is chosen. With the improved Miller compensation techniques, the compensation capacitance can be reduced, then the slew rate can be also improved without increasing the bias current. Especially for voltage follower configuration, it is realized that the compensation capacitor does not limit the slew rate in principle. The bias current can be further reduced with this compensation. In fast-settling discrete-time applications and high frequency filters, the introduction of zero is suitable for low power. In the LCD column driver, the phase compensation by using the zero formed with a load capacitance is effective for power reduction. In high cut-off frequency active-RC filters, the opamp with no capacitor feedforward phase compensation dissipates lower power than the opamp with the Miller compensation. These techniques are suitable for low power and/or wideband opamps.

References


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