Niobium-Silicide Junction Technology for Superconducting Digital Electronics*

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SUMMARY We present a technology based on Nb/NbxSi1−x/Nb junctions, with barriers near the metal-insulator transition, for applications in superconducting electronics (SCE) as an alternative to Nb/AIOx/Nb tunnel junctions. Josephson junctions with co-sputtered amorphous Nb-Si barriers can be made with a wide variety of electrical properties: critical current density (Jc), capacitance (C), and normal resistance (Rn) can be reliably selected within wide ranges by choosing both the barrier thickness and Nb concentration. Nonhysteretic Nb/NbxSi1−x/Nb junctions with JcRn products greater than 1 mV, where Ic is the critical current, and Jc values near 100 kA/cm² have been fabricated and are promising for superconducting digital electronics. These barriers have thicknesses of several nanometers; this improves fabrication reproducibility and junction uniformity, both of which are necessary for complex digital circuits. Recent improvements to our deposition system have allowed us to obtain better uniformity across the wafer.

key words: amorphous alloy, Josephson device fabrication, Josephson junctions, superconducting devices

1. Introduction

Digital Superconducting Electronics (SCE), which has the potential for lower power consumption and faster switching speeds compared to some semiconductor technologies, is a promising technology to deliver ultra-high performance computation. The earliest SCE circuits used junctions with lead and lead alloys, but these suffered from poor stability and their properties deteriorated after repeated thermal cycling. Presently, the preferred technology for high-speed superconductive digital circuits, which was developed in the early 1980’s, is based on Nb/AIOx/Nb junctions with barrier thicknesses on the order of 1 nm [1]. These junctions have proved to be stable, reproducible, and able to yield uniform devices.

Important developments have been achieved using this technology; some of the most impressive achievements include a T-flip-flop circuit operating up to 770 GHz [2] and a 4 kbit memory operated at 580 ps and 6.7 mW [3]. For the highest speed and density, circuits rely on high critical current density (Jc) junctions and submicrometer junction dimensions. Tunneling Nb/AIOx/Nb junctions are hysteretic and need shunting resistors to bring them to the critically damped regime, limiting the circuit density and introducing parasitic inductances. Only very high Jc Nb/AIOx/Nb junctions (> 200 kA/cm²) [4] with deep sub-micron dimensions are self-shunted due to their very thin oxide barriers, one or two monolayers thick. Self-shunting in this case is due to metallic micro-shorts across the barrier [5]. For these junctions, Jc uniformity is much more difficult to achieve and may be inherently limited by the random distribution of micro-shorts.

Other attempts have been made to obtain suitable junctions for SCE, with high Jc and no hysteresis, including SINIS [6] and SNIS [7] (S=superconductor, I=insulator, N=normal metal) junction technologies, with Al and AIOx as normal metals and insulators, respectively. AlN has been evaluated as a barrier material [8] as have SNS junctions with high-resistivity barrier materials such as TiN [9], NbN [10] and TaN [11], for which the resistivity is changed according to the nitrogen concentration and substrate temperature. The only technology that has been partially competitive with Nb/AIOx/Nb has been NbN-based junctions with various barriers, with the higher transition temperature superconducting NbN, having the advantage of circuit operation near 10 K [12].

We propose an alternative technology for SCE based on Nb/NbxSi1−x/Nb junctions. By choosing x ≤ 0.05, the Nb-Si barriers can be reproducibly tuned between metallic and insulating behavior [13]. A junction with a several-nanometer thick Nb-Si barrier would produce comparable electrical performance to that of high-Jc tunnel junctions, but has the potential for better reproducibility and uniformity.

2. Fabrication of Nb/NbxSi1−x/Nb Junctions

NIST has been developing Nb/NbxSi1−x/Nb junctions to replace previously successful junction technologies for voltage standards, most notably PdAu and MoSi2 barrier SNS junctions. Typically, these junctions have a low normal resistance Rn and, as a consequence, low values of IcRn (if Ic is to be kept within practical limits). This makes them unsuitable for high-speed electronics. However, unlike tunneling junctions, whose electrical properties are tuned by the oxygen exposure, which defines the barrier thickness, in Nb/NbxSi1−x/Nb junctions two controllable parameters, thickness and composition of the barrier, determine the junction’s properties [14]. The control of the composition is achieved through the co-sputtering of Nb and Si as shown in Fig. 1.

While the deposition time and rate determine the thick-
Fig. 1 Cosputtering allows for control of barrier composition as well as thickness, enabling junctions with a wide variety of properties.

Fig. 2 $I_cR_n$ vs. barrier thickness for Nb/Nb$_x$Si$_{1-x}$/Nb junctions with different Nb content in the barrier determined by the power of the Nb sputtering gun. The Si sputtering gun power was set at 200 W for all junctions in the figure.

ness, the composition is determined by the relative powers of the Nb and Si sputtering guns. This allows a continuous spectrum of barrier properties from low resistance, Nb-rich barriers, to insulating barriers of pure silicon. Within a wide range of possible values, $J_c$ and $R_n$ can be reliably and independently selected, giving junctions of varied characteristics. Of particular interest for SCE are junctions with thin barriers in the insulating regime, which have $I_cR_n$ products greater than 1 mV and $J_c$ near 100 kA/cm$^2$. These junctions are more robust than SINIS (S=superconductor, I=insulator, N=normal metal) junctions that have AlO$_x$ for the insulator, which have also been used in voltage standard applications. SINIS junctions seem to be affected by plasma processing, giving a low yield of working devices [17]. Junctions with Nb-Si barriers, on the other hand, are more robust, due in part to the increased thickness of the barriers, which is of the order of several nanometers.

In our system, a three-inch diameter silicon wafer substrate with 150 nm of silicon oxide is held against a rotating platen located at approximately 15 cm from the sputtering targets. The platen is cooled with flowing nitrogen gas and a heat sinking film or plate is placed at the back of the wafer against the platen. Patterning of junctions is done by reactive ion etching in a mixture of SF$_6$ and C$_4$F$_8$, giving an excellent vertical profile and allowing for the fabrication of uniform vertical stacks of junctions [15]. Silicon oxide insulation is deposited by electron cyclotron resonance (ECR) plasma-enhanced chemical vapor deposition, giving a low-stress, high quality oxide. Vias through the oxide are done by reactive ion etching in a mixture of O$_2$ and CHF$_3$.

To improve the uniformity of the junctions, an Argon plasma etch is applied to the base electrode and, in the case of vertical stacks, each middle electrode. This process smooths the Nb surface prior to the barrier deposition. In the case of thin barriers, a rough surface would contribute to non-uniformities in $J_c$. Roughness particularly affects stacks because it accumulates as the stacks grow vertically [16]. A good etching profile of stacked junctions allows for uniform properties with potential for high-density vertical stacks of junctions for application in output circuits with very small parasitic inductances.

3. Junction Properties

Josephson junctions made with co-sputtered Nb-Si barriers have already been shown to have excellent uniformity and reproducibility in Josephson voltage systems in which tens of thousands of junctions all have sufficiently similar properties to each other in order for 10 V to be obtained from the addition of their first constant voltage step under microwave bias. These junctions are more robust than SINIS (S=superconductor, I=insulator, N=normal metal) junctions that have AlO$_x$ for the insulator, which have also been used in voltage standard applications. SINIS junctions seem to be affected by plasma processing, giving a low yield of working devices [17]. Junctions with Nb-Si barriers, on the other hand, are more robust, due in part to the increased thickness of the barriers, which is of the order of several nanometers. For voltage standards, it has been straightforward to change the characteristic frequency of junctions from 20 GHz to 70 GHz by choosing the appropriate composition and thickness. Excellent uniformity was demonstrated with large circuits of ~70000 nearly identical junctions [17]. Similarly, much faster junctions suitable for SCE with characteristic frequencies above 500 GHz have also been fabricated [18].

An important and desired feature of any junction technology for applications in SCE is the reproducibility of junction properties. For our junctions this can be seen in the dependence of $J_c$ on barrier composition and thickness, as demonstrated in Ref. 16. For a fixed barrier composition, $J_c$ has a nearly exponential dependence on the barrier thickness. This allows us to accurately target the properties of the junctions according to the desired application.

High values of $I_cR_n$ can be achieved with a variety of thickness and composition combinations. More metallic barriers produce large values of $J_c$, which require smaller lateral fabrication dimensions to maintain practical $I_c$ values. These junctions are ideally suited for SCE logic, because they are intrinsically critically damped, as shown in Fig. 3. Without the need for shunt resistors, they avoid the parasitic inductances arising from shunts and can achieve...
higher circuit density. More resistive barriers will allow larger lateral junction dimensions, but the reduced damping will increase their hysteresis. Hysteretic junctions are suitable for latching logic and output circuits, such as Suzuki stacks [19].

The simultaneous but independent control of composition and thickness allows us to obtain junctions with a chosen \( J_c \) but different composition and thickness, so that they have different characteristic frequencies and a different amount of damping, which produces different magnitudes of hysteresis in the current-voltage curves (IVC). As an example, Fig. 4 shows a set of six IVC for pairs of parallel junctions with dimensions of 2.5 \( \mu \text{m} \times 2.5 \mu \text{m} \). The junction pairs have different composition and thicknesses, but are all designed to have the same value of \( J_c \). As the concentration of Nb decreases, the junctions become more resistive and also more hysteretic, because the less metallic barriers become more resistive. The preferred properties for a specific application can be obtained through the correct choice of thickness and composition. For high-speed digital electronics, for example, high values of \( \frac{I_c}{R_n} \) can be achieved with a variety of combinations of thickness and composition.

Table 1 shows the growth conditions and measured properties of junctions with different barriers (from different wafers), including \( J_c \), capacitance \( C \), amount of hysteresis \( I_{ret} \), and dielectric constant \( \epsilon \) of the barrier. Capacitances were inferred by measuring voltage resonance steps in the IVC of SQUIDs in which flux was coupled by adjusting the current in a directly coupled wire, as described in [20]. The values of \( C \) and \( \epsilon \) decrease as the Nb content of the barrier decreases. Figure 5 shows these trends for the same group of wafers with similar \( J_c \), as in Fig. 4.

In Fig. 3, we can see that the value of the resistance in the sub-gap region \( (R_{sg}) \) near to \( I_c \) is considerably larger than \( R_n \) (the resistance above the superconductor gap voltage). Consequently, \( I_c R_{sg} \) is much larger than \( I_c R_n \). This value of \( I_c R_{sg} \) may be more representative of the speed of
the junction, as it is the value in the region close to the operation point of the junction. Likewise, based on capacitance measurements, for the IVCs in Fig. 4 with little or no hysteresis, the expected value of damping parameter $\beta$ should be around and not much bigger than 1. If we use the values of $R_{sp}$ near $I_c$ and the calculated capacitances from voltage resonance steps, the values for $\beta$, obtained are 1.3 (for 16/200 W) and 2 (for 15/200 W), compared to values a factor of ten smaller when $R_{sp}$ is used. This suggests also that the value of $R_{sp}$ near $I_c$ better represents the junction dynamics and also suggests faster operation than that given by the $I_c/R_{sp}$ values in Fig. 2 [21].

4. Improvements in Deposition Conditions

It has been found that junctions having barriers with low Nb content are particularly susceptible to residual impurity gases in the chamber during deposition. Voltage standard circuits operating at 75 GHz were found to have large $J_c$ non-uniformity across the wafer [22]. The origin of the non-uniformity was found to be outgassing from the cooling graphite foil (used to heat-sink the wafer during deposition) and possibly also the platen in back of the wafer. The effect was more pronounced in circuits that were located nearest to the flat of the wafer, where there was a small opening in the wafer holder. A new holder plate with no gap improved the uniformity. Experiments on thicker films made of only the barrier material showed considerable improvement in resistivity uniformity after a new “gapless” holder plate was installed. Before this change, a film deposited with 8/200 W (Nb/Si power) had a mean resistivity of 7.4 m$\Omega$-cm with a standard deviation of 5.6 m$\Omega$-cm. After removing the gap and reducing the residual gases, a wafer with similar junction deposition conditions had less than half the average resistivity (3 m$\Omega$-cm) and more than 10-times lower standard deviation (0.4 m$\Omega$-cm). A further increase in $J_c$ and decrease of barrier resistivity was obtained by replacing the graphite foil with a solid Al metallic disc for wafer cooling. Unfortunately, it was unclear which residual gas was responsible for the depressed value of $J_c$. Preliminary studies show that it is also possible that residual water vapor may be responsible for suppression of the critical current density.

As expected, the value of $J_c$ increases either as the Nb content increases or the barrier thickness decreases. $J_c$ also increases when the material impurities in the barrier are reduced. The last five entries of Table 1 show samples with the same composition and thickness; they all have similar values of $C$ and $\epsilon$, but those near the bottom, corresponding to improvements in wafer mounting in the deposition chamber, have higher $J_c$ and, at the same time, less hysteresis. Future work will evaluate the reproducibility of the electrical properties under these deposition conditions.

5. Conclusion

We have shown that the versatility of co-sputtered Nb/Nb$_x$Si$_{1-x}$/Nb junctions permits the fabrication of junctions with electrical properties suitable for SCE. Their fabrication is similar to existing technologies, with only the minor modification of cosputtering the barrier. The junctions have been shown to be reproducible and uniform. Work is presently underway on the fabrication and testing of simple digital superconducting circuits based on these junctions.

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References


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Samuel P. Benz was born in Dubuque, IA, on December 4, 1962. He received the B.A. degree (summa cum laude) in physics and math from Luther College, Decorah, IA, in 1985 and the M.A. and Ph.D. degrees in physics from Harvard University, Cambridge, MA, in 1987 and 1990, respectively. He was awarded an R.J. McElroy Fellowship (1985–1988) to work toward the Ph.D. degree. In 1990, he joined the National Institute of Standards and Technology (NIST), Boulder, CO, as a NIST/NRC Postdoctoral Fellow and became a permanent Staff Member in January 1992. He has been the Project Leader of the Quantum Voltage Project at NIST since October 1999. He has worked on a broad range of topics within the field of superconducting electronics, including Josephson junction array oscillators, single flux quantum logic, ac and dc Josephson voltage standards, and Josephson waveform synthesis. He has 150 publications and is the holder of three patents in the field of superconducting electronics. Dr. Benz is a member of Phi Beta Kappa and Sigma Pi Sigma. He was the recipient of two U.S. Department of Commerce Gold Medals for Distinguished Achievement.